CS301ES: ANALOG AND DIGITAL ELECTRONICS

B.TECH II Year I Sem.

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Course Objectives:

- To introduce components such as diodes, BJTs and FETs.
- To know the applications of components.
- To give understanding of various types of amplifier circuits
- To learn basic techniques for the design of digital circuits and fundamental concepts used inthe design of digital systems.
- To understand the concepts of combinational logic circuits and sequential circuits.

Course Outcomes: Upon completion of the Course, the students will be able to:

- Know the characteristics of various components.
- Understand the utilization of components.
- Design and analyze small signal amplifier circuits.
- Learn Postulates of Boolean algebra and to minimize combinational functions
- Design and analyze combinational and sequential circuits
- Know about the logic families and realization of logic gates.

UNIT - I

Diodes and Applications: Junction diode characteristics: Open circuited p-n junction, p-n junction as a rectifier, V-I characteristics, effect of temperature, diode resistance, diffusion capacitance, diode switching times, breakdown diodes, Tunnel diodes, photo diode, LED.

Diode Applications - clipping circuits, comparators, Half wave rectifier, Full wave rectifier, rectifier with capacitor filter.

UNIT - II

BJTs: Transistor characteristics: The junction transistor, transistor as an amplifier, CB, CE, CC configurations, comparison of transistor configurations, the operating point, self-bias or Emitter bias, bias compensation, thermal runaway and stability, transistor at low frequencies, CE amplifier response, gain bandwidth product, Emitter follower, RC coupled amplifier, two cascaded CE and multi stage CE amplifiers.

UNIT - III

FETs and Digital Circuits: FETs: JFET, V-I characteristics, MOSFET, low frequency CS and CD amplifiers, CS and CD amplifiers.

Digital Circuits: Digital (binary) operations of a system, OR gate, AND gate, NOT, EXCLUSIVE OR gate, De Morgan Laws, NAND and NOR DTL gates, modified DTL gates, HTL and TTL gates, output stages, RTL and DCTL, CMOS, Comparison of logic families.

UNIT - IV

Combinational Logic Circuits: Basic Theorems and Properties of Boolean Algebra, Canonical and Standard Forms, Digital Logic Gates, The Map Method, Product-of-Sums Simplification, Don't-Care Conditions, NAND and NOR Implementation, Exclusive-OR Function, Binary Adder-Subtractor, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers.

UNIT - V

Sequential Logic Circuits: Sequential Circuits, Storage Elements: Latches and flip flops, Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Shift Registers, Ripple Counters, Synchronous Counters, Random-Access Memory, Read-Only Memory.

TEXTBOOKS:

1. Integrated Electronics: Analog and Digital Circuits and Systems, 2/e, Jaccob Millman, Christos Halkias and Chethan D. Parikh, *Tata McGraw-Hill Education*, India, 2010.
2. Digital Design, 5/e, Morris Mano and Michael D. Cilette, *Pearson,* 2011.

REFERENCE BOOKS:

1. Electronic Devices and Circuits, Jimmy J Cathey, *Schaum's outline series*, 1988.
2. Digital Principles, 3/e, Roger L. Tokheim, *Schaum's outline series*, 1994.

Electron: It is Negatively charged Sub-atomic particles

Electronics: It is nothing but Study of the electron under the influence of the electron and Magnetic field.

Current: The flow of electrons is nothing but "current".

Voltage: The potential difference between the 2 points

$V_1 \rightarrow V_2$

$V_0 = V_1 - V_2$

Classification of material :⇒

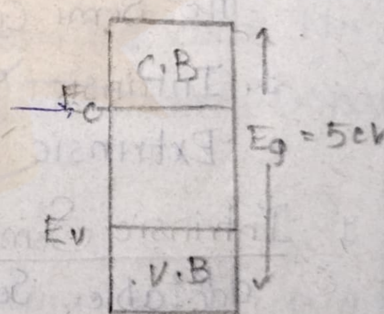
Based on the energy band gap the materials are classified into 3 types.

1. Insulators
2. Conductors
3. Semiconductors.

Insulator :⇒ It is a bad conductor of Electricity.

Eg: Paper, rubber, wood etc..,

→ The energy gap for the insulator is



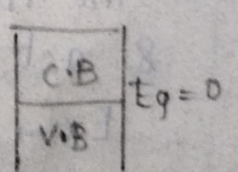
→ Diamond is a good insulator because energy gap is greater than 6eV

→ Ionic bond existed.

Conductor :⇒

It is a good carrier for electricity.

Ex: All metals.



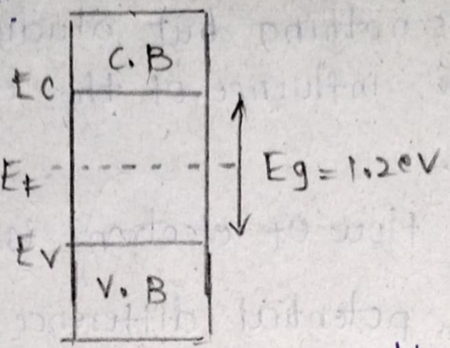
→ The metallic bond exist in conductance.

→ The energy gap is equal to zero in conductors.

→ As the temperature ↑ energy gap ↓, that means the valency bond is overlapped with conduction bond.

Semi conductors:⇒

The semiconductors energy gap is greater than 1eV or less than 2eV.



→ The semiconductor electrical properties lies b/w insulator and conductor.

→ The semiconductor conductivity is greater than the insulator and less than the conductors.

→ The resistivity of Semi conductor is less than the insulator and greater than the conductor.

→ As temperature ↑es the energy gap is ↓es vice versa.

$$\downarrow E_G \propto \frac{1}{T} \uparrow$$

→ The Semi Conductors are classified into 2 types

1. Intrinsic Semi Conductor
2. Extrinsic Semi Conductor.

1. **Intrinsic Semiconductor:⇒** It is a pure and non-detectable Semiconductors in this electron concentration is equal to hole concentration.

→ The intrinsic Semi Conductor acts as a insulator at 0 kelv & act as conductor at 300K.

Ex:→ Pure Silicon, Pure Germanium.

→ The conductivity due to electrons and holes.

Extrinsic Semiconductor:→ By adding some impurities to the intrinsic semiconductor we can form extrinsic Semiconductor.

Intrinsic Semiconductor + Impurity = Extrinsic Semiconductor.

→ The process of adding impurities is called "doping".

→ The extrinsic semiconductor are divided into 2 types depending on the doping.

1. N-type Extrinsic Semi Conductor :→

By adding Vth group elements to the intrinsic Semi-Conductor we can form N-type Semi Conductors.

→ The Vth group elements are Phosporous, Arsenic, Antimony & Bismuth.

→ In N-type Semi Conductors the majority charge carriers are electrons & minority charge carriers are holes.

→ In N-type Semi Conductors is represented with N_D.

→ The N-type Semi Conductors are also called "Donars"

2. P-type Extrinsic Semi Conductor:→

P-type Semiconductor is formed by adding IIIrd group elements to the intrinsic semiconductor.

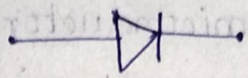
→ The IIIrd group elements are B, Al, Ga, In, Tl.

→ The P-type Semiconductor the whole concentration will be represented with "N_A". The P-type Semiconductor is also called as Acceptor.

→ In P-type Semiconductor the majority charge carriers are holes & minority charge carriers are electrons.

P-N Junction diode:→

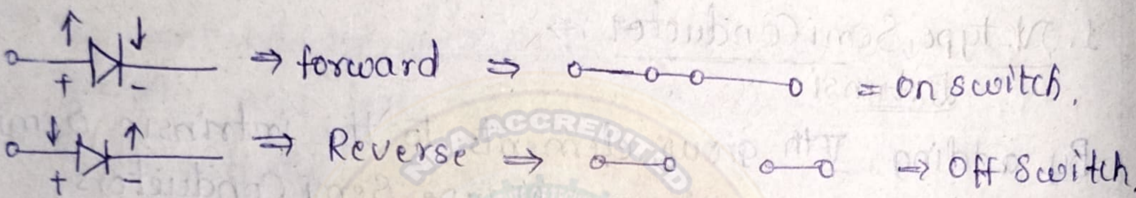
→ It is a 2 terminal & Unidirectional device.

→ The Symbol for the diode is 

→ The p-n junction diode will operate in 2 types of biases, 1. Forward bias. 2. Reverse bias.

→ In Fordward Bias mode it will be worked as an on Switch.

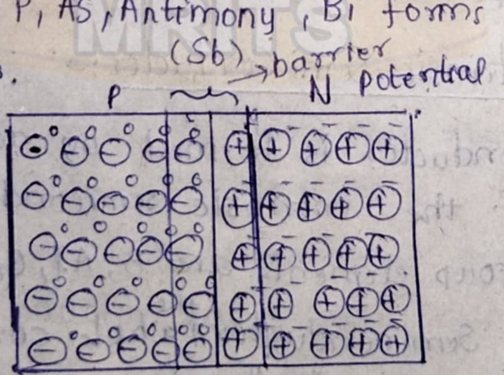
→ In Reverse Bias mode, it will be worked as off Switch



Construction:→

One Semiconductor material is doping with Vth group elements to one side and the another side doping with IIIrd group elements. We can form a p-n junction diode.

→ The IIIrd group elements like Boron, Aluminium, gallium, Indium, Thalium forms the p-type, the Vth group elements are P, AS, Antimony (Sb), Bi forms the n-type Semiconductors.



→ In P-type Semiconductor the majority charge carriers are holes and minority charge carriers are electrons.

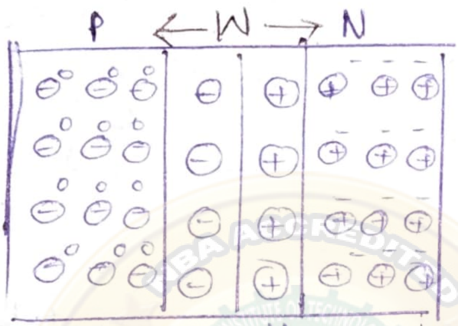
→ In N-type Semicondutor the majority Charge carriers are electrons & minority charge carrers are holes.

→ In open circuit p-n junction because of concentration difference the holes attracted by the electrons and the electrons attracted by the holes. ~~Because of~~ Therefore the hole will recombine with electron & it forms and immobile ions at the junction.

→ The immobile ions will form a charge by integrating the charge we get the voltage. This voltage called contact potential or Barrier potential or ~~Cutting~~ Voltage. .cut-in

→ The Cut-in Voltage for Silicon is 0.6 – 0.7V.

→ The Cut-in Voltage for Germanium is 0.2 – 0.3V



→ The electron & hole recombination occur until the equilibrium ~~condition~~ condition (condition)
No further recombination from e⁻ to hole & viceversa.

→ Because of Immobile ions some region is depleted that region is called depletion region (or) Space-charge region. have only charge do not have speed

→ The depletion width for a normal pn junction diode is 0.1 μm – 1 μm.

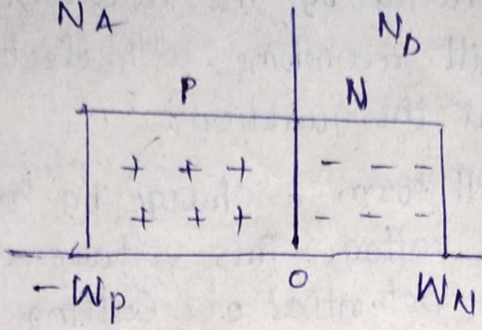
→ The charge developed across the junction is depend on the width of the depletion region & the charge developed due to the holes is given by $\rho = -N_A q$

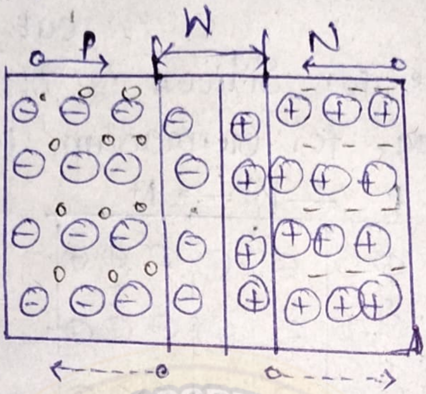
→ The charge developed due to the ~~holes~~ electron is $N_D q$

→ The depletion width is depending on the doping concentration. $W \propto \sqrt{\frac{1}{N_A} + \frac{1}{N_D}}$

→ The potential developed across the junction is given by

$$V_0 = \sqrt{\frac{2E}{q} V_0 \left[\frac{1}{N_A} + \frac{1}{N_D}\right]}$$





←o → Diffusion current due to e⁻

o - - -→ → " " " Holes

⟵o → Drift " " " e⁻'s

o - - -→ → Drift " " " Holes.

Diffusion Current :⇒

The Current which is due to the diffusion of carrier because of concentration gradient or density difference then it is called diffusion current.

→ Diffusion Current density is directly proportional to the concentration gradient.

$$\boxed{\frac{dn}{dx} = \frac{n_2 - n_1}{x_2 - x_1}}$$

$$\boxed{\frac{dp}{dx} = \frac{p_2 - p_1}{x_2 - x_1}}$$

→ The diffusion current due to the holes is

$$\boxed{I_p = -q D_p \frac{dp}{dx}}$$

$$\boxed{I_n = -q D_n \frac{dn}{dx}}$$

Drift Current:⇒ The current is due to the drifting of carriers because of applied Electric field is called drift current.

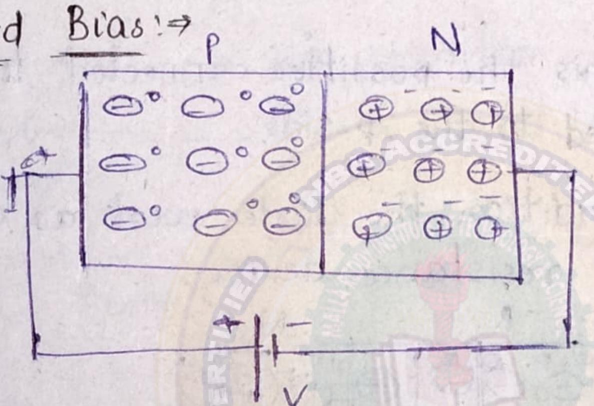
→ The current is nothing but flow of e⁻'s (or) charge carriers if the charge carriers is due to applied Electric field then it is called drift current.

→ Drift current due to the holes is $I_p = pq\mu_p A$

→ " " due to the electrons is $I_n = nq\mu_n A$

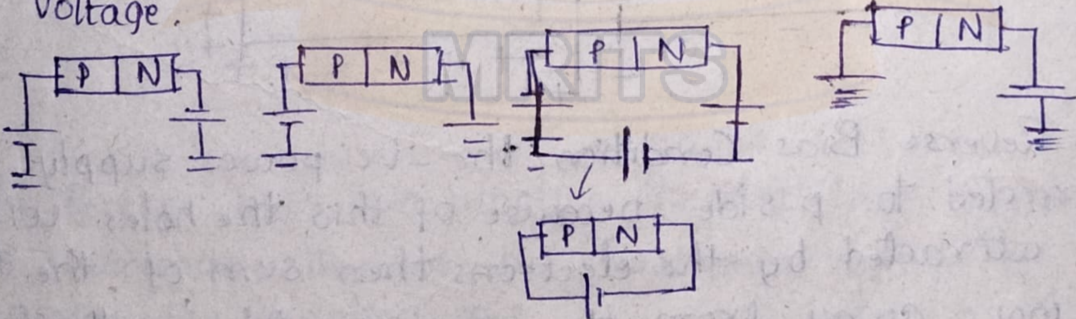
→ The p-n junction diode opereated in 2 modes one is Forward bias & Reverse bias.

Fordward Bias:⇒



→ In this bias the positive terminal is connected is pside & Negative is connected to n-side.

→ When p-n junction is forward bias the junction voltage is reduces and also it is lesser than the forward bias voltage.



~~Reverse bias:⇒~~

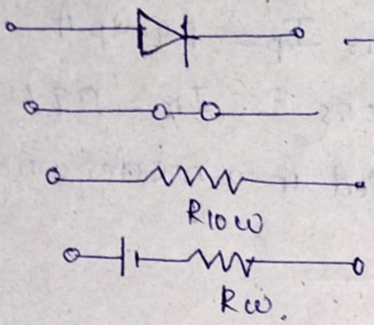
→ In Forward Bias the junction width is depends on the doping concentration & temperature.

→ If the temperature ↑'es the junction width ↓'es vice versa

→ In forward bias p-n junction diode the cutting voltage for Silicon is 0.6 (or) 0.7 V for Germanium is 0.2 (or) 0.3 V.

→ The junction voltage (or) Cutting voltage for forward bias in pn junction diode is $V_0 = \sqrt{\frac{2E}{q}(V_j - V)\left[\frac{1}{N_A} + \frac{1}{N_D}\right]}$

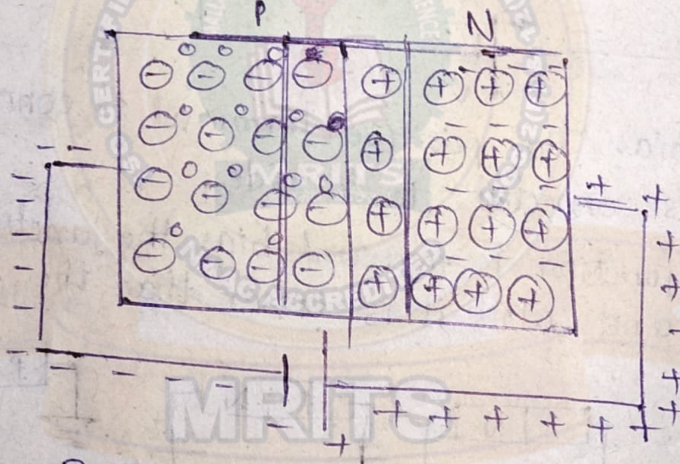
→ In forward bias condition the diode is in short circuit & it will be work as an on Switch.



→ Symbol
→ F.B condition.
→ Linear mode (Practical mode)
→ piece wise Linear Model.

Reverse Bias :⇒ In this the possitive connected to n-side & negative connected to the p-side.

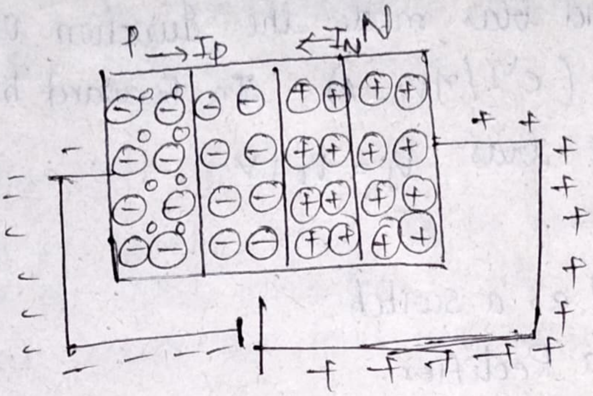
→ In Reverse bias condition the diode work as an off Switch i.e High resistance device.

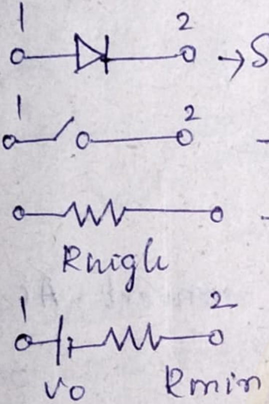


→ In Reverse Bias Condition the -ve power supply connected to p-side because of this the holes will get attracted by the electrons then sum of the holes will move away from the junction. At another side the electrons will get attracted by the holes. Because of this reason the electron also will move away from the junction. Therefore no charges present across the junction i.e the junction width is increased.

→ Due to the larger width no carrier will move towards the junction.

→ Therefore no current due to the majority charge carriers but some current is exist due to minority charge current that current called as Leakage current.



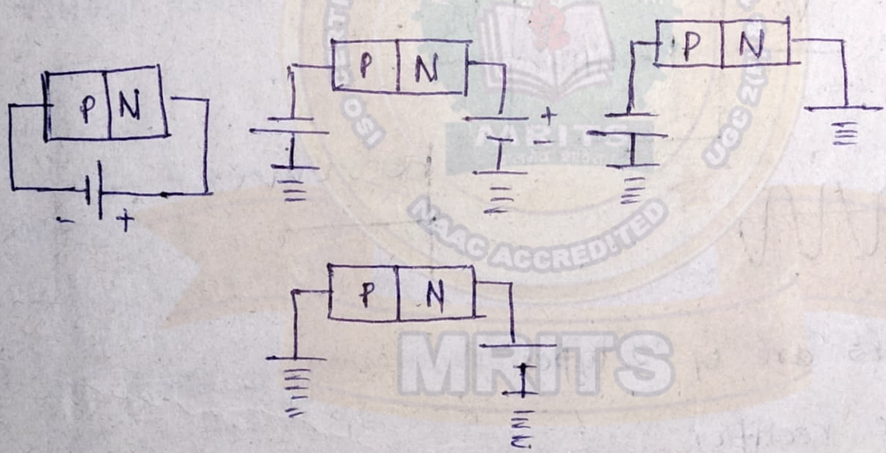


→ Symbol

→ R.B condition.

→ linear Model (practical)

→ piece wise linear Model.



In Reverse bias p-n junction the depletion region/width is maximum. Therefore the maximum voltage is existed across the junction. ~~In~~

→ Generally the diode current Equation is given by

$$I = I_0 \left(e^{V/\eta V_T} - 1 \right)$$

I = diode Current.

I_0 = Leakage current

V = Voltage across the junction

V_T = Thermal voltage i.e $\frac{T}{11,600}$

η = 1 for Germanium & 2 for Silicon

Generally

→ In Forward bias mode the Junction voltage is equal to $I = I_0 (e^{V_j/\eta V_T} - 1)$ In Forward bias $V_j = V_0 - V$

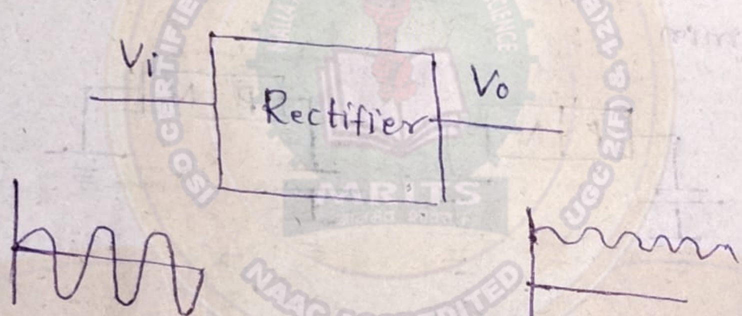
→ In Reverse bias $V_j = V_0 + V$

Applications:⇒

1) It is used as a switch.
2) Used as a Rectifier.
3) Clippers → cut
4) Clampers. → hold
5) ~~Multi vib~~

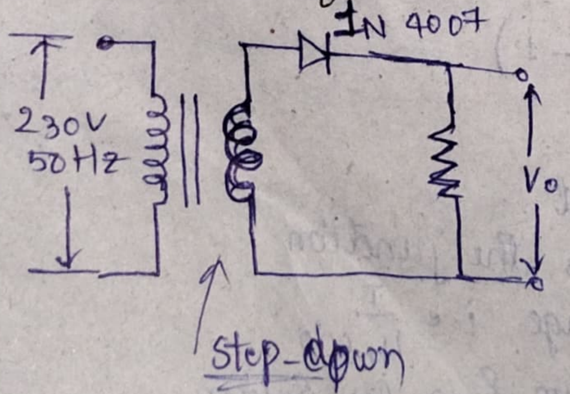
Rectifiers:⇒ V.V Imp.

The purpose of the rectifier is ~~used~~ to convert AC to pulsating DC



The rectifiers are of 2 types
1. Half wave rectifier
2. Full wave rectifier.
   I. Centre tapped full wave rectifer
   II. Bridge Rectifier.

1. Half Wave Rectifier :⇒ (without filter)



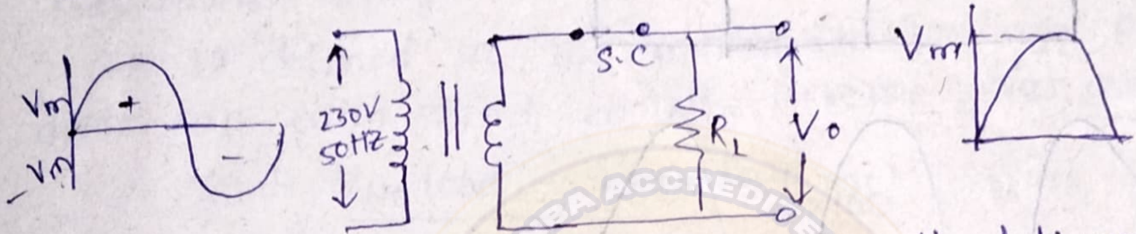
Construction:→

The connection of the half wave rectifier has shown above. In this one step down transformer, one PN Junction diode, 1 load resistor is used. Across the load resistor the output is taken.

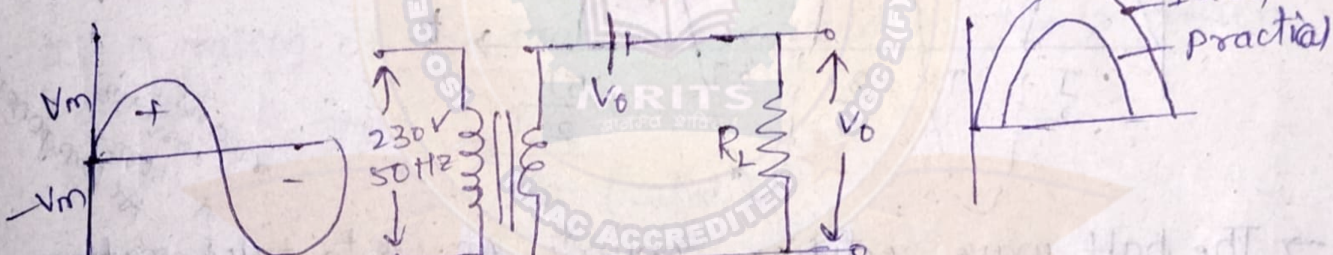
Operation:→

During the positive Half Cycle:→

In this case the p-n junction diode is in forward Bias that means it is short circuited i.e the total current will be delivered across the load resistance (R_L)



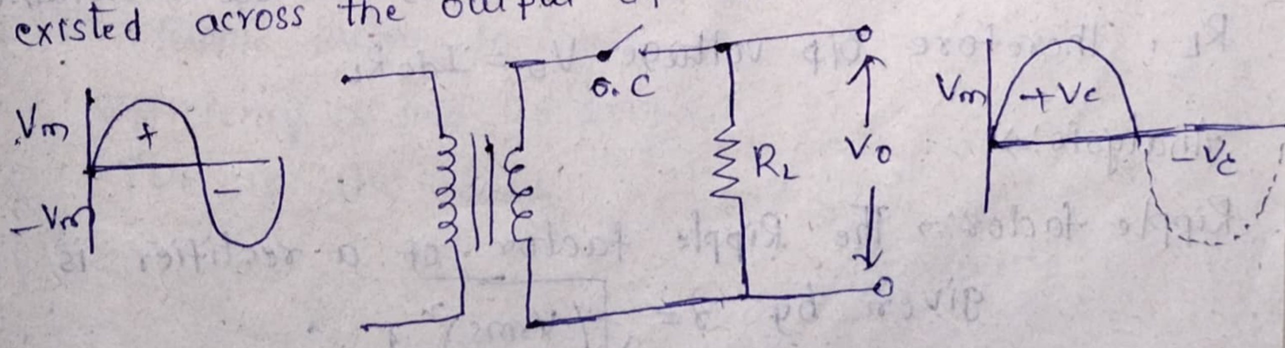
→ In Ideal case the total Voltage will delivered across the Load resistor (R_L) but in practical case some voltage drop existed across the diode.



→ In Forward bias condition the diode acts like a on Switch.

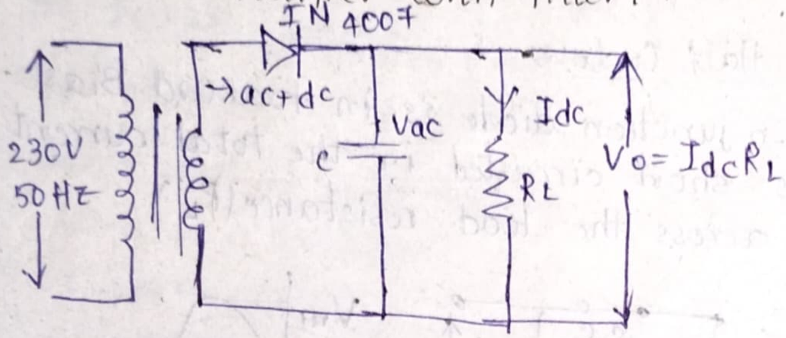
During the Negative Half Cycle:→

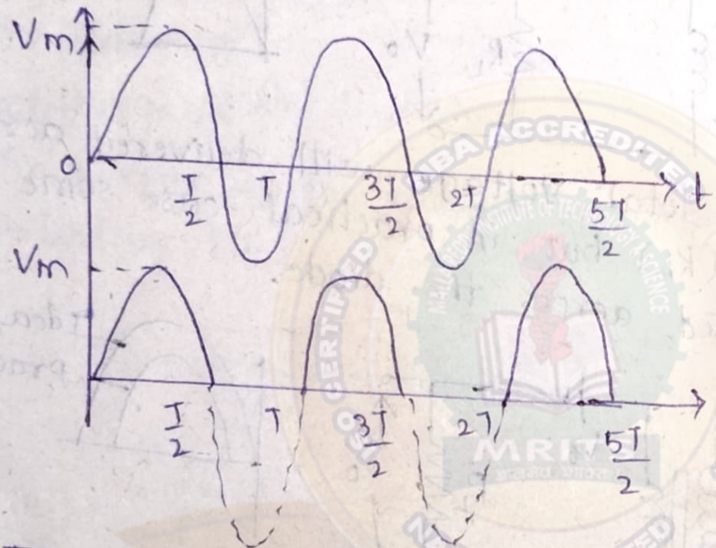
In this case the diode is in reverse bias that means it acts like a open circuit, no current will travel to the load resistor (R_L) & Hence no voltage existed across the output of the diode.



→ Ideally voltage drop across the Load resistor is "zero" but practically some Leakage current is travelled towards the R_L i.e nothing but output voltage.

Half-wave rectifier with filter :⇒





means contain some AC component

→ The half wave rectifier converts AC into pulsating DC that means some noise components are existed with the DC. That noise components are abided by using a filter current. That filter circuit is a capacitor. It is abided all the noise components existed in the output signal.

→ The pure DC will travel towards the low resistance R_L. Therefore O/P voltage $V_0 = I_{dc} R_L$

Analysis :⇒

Ripple factor :⇒ The Ripple factor of a rectifier is given by $\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$

→ The Ripple factor for half-wave rectifier is given by

$V_\gamma = 1.21$.

Efficiency :→ It is defined as the ratio of DC o/p power to the AC I/p power

$$\% \eta = \frac{P_{dc}}{P_{ac}} \times 100$$

→ The efficiency for Half wave rectifier is 40.6%

Peak Inverse Voltage:

It is defined as the maximam voltage of a diode can with stand in its reverse bias condition

$$\% = \frac{V_{No\ load} - V_{FULL\ load}}{V_{FULL\ load}} \times 100$$

$$\boxed{PIV = V_m}$$

Transformer utilisation Factor:→

It is rating of the transformer used in the rectifiers circuit

$$TUF = \frac{P_{dc}}{P_{ac}\ (rated)}$$

Form factor = 1.57

Peak factor = 2

$$\Rightarrow V_{dc} = \frac{V_m}{\pi} \quad I_{dc} = \frac{I_m}{\pi R_L}$$

$$\Rightarrow I_{rms} = \frac{I_m}{2} \quad V_{rms} = \frac{V_m}{2}$$

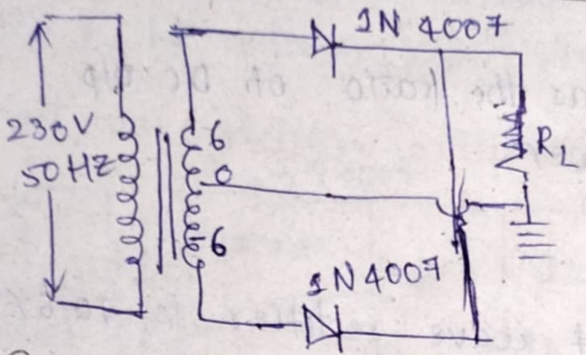
Disadvantages:→

1. The Ripple factor is low
2. Efficiency is low i.e 40.6%.
3. TUF is also Low.

Full wave rectifier (F.W.R) (Centre trapped F.W.R)

Filter = capacitor

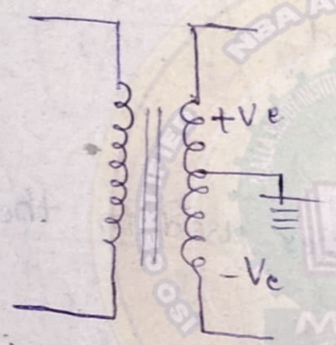
(without filter)



Construction:→

In this one Center trapped transformer is required, 2 diodes and 1 load resistor is required.

→ The Center trapped transformer splitted the voltage into 2 parts



Operation:→

During the positive half cycle:→

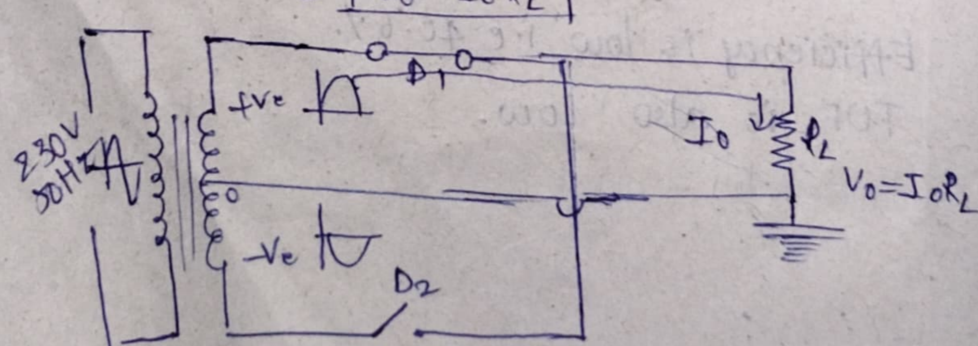
→ By using the Center tapped transformer the +ve half cycle will splitted into 2 portions at diode D_1 it is +ve at diode D_2 it is -ve.

→ The diode D_1 is forward biased because of +ve voltage.

→ the diode D_2 is reverse biased because of -ve voltage.

→ The total current will delievered at the across the load resistor via 'D_1'.

→ The total voltage R_L $V_0 = I_0 R_L$



→ In ideal case the total voltage will delivered across the R_L. But in practically some voltage drop existed across the diode junction.

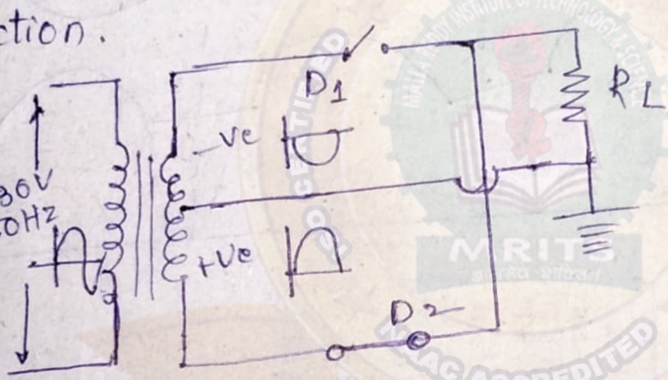
→ The diode D_2 in open circuit condition i.e it acts as a OFF switch.

<u>During the Negative half Cycle</u>:→

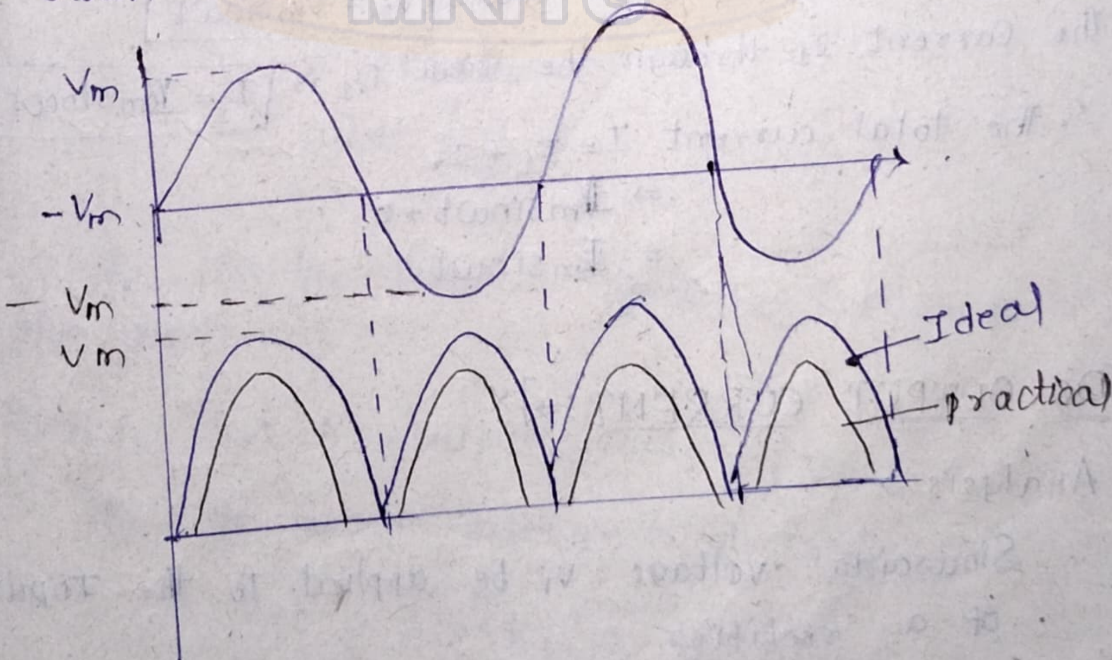
→ In this case the diode D_1 is reverse biased because of Negative power supply and the diode D_2 is forward biased because of positive power supply.

→ The total current will deliever across the Load resistor R_L Via/through D_2.

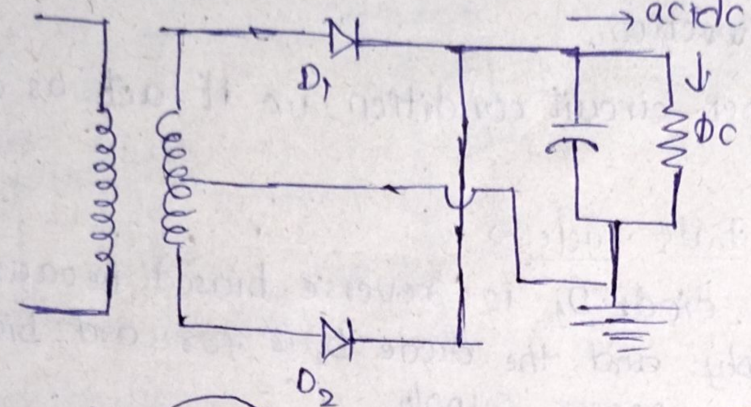
→ In Ideal the total voltage will appear across the R_L but in practical Some voltage is existed across the junction.

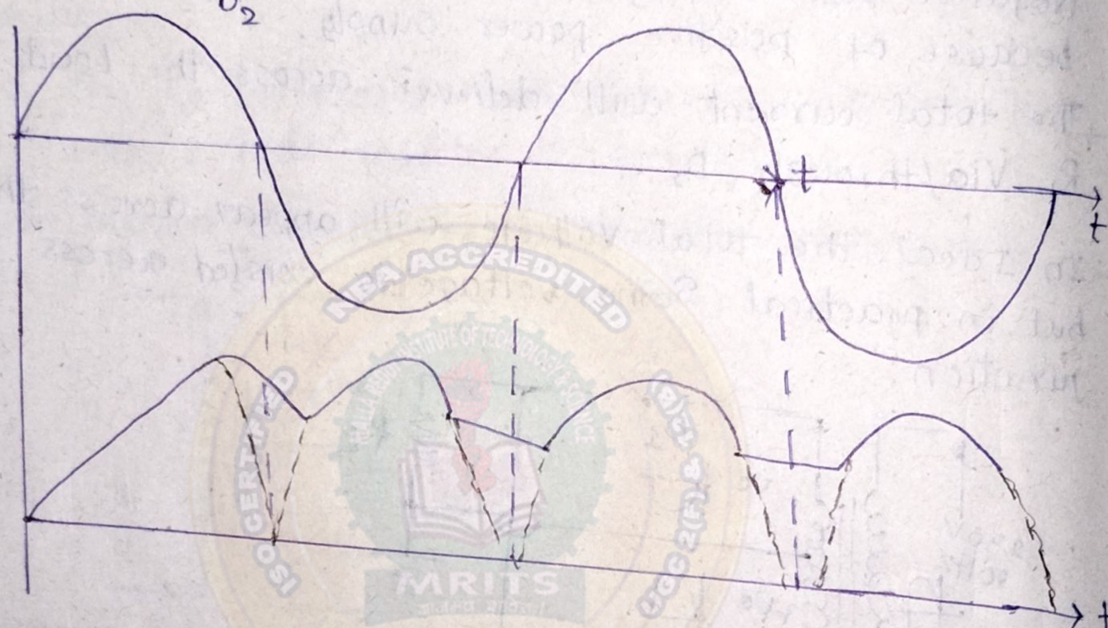


→ The output wave form for the full wave rectifier as shown below



Full wave rectifier (With filter)





Analysis:⇒

→ The sinusoidal input is applied to the rectifier

→ The input voltage is given that $v_i = V_m \sin\omega t$

→ The Current I_1 through the diode D_1 is $I_1 = I_m \sin\omega t$ $0 < t < \frac{\pi}{2}$

∴ The total current $I = I_1 + I_2$

$$\Rightarrow I_m \sin\omega t + 0$$

$$= I_m \sin\omega t$$

I

DC OUTPUT CURRENT:⇒

Analysis:⇒

Sinusoidal voltage v_i be applied to the Input of a rectifier

i.e $v_i = V_m \sin\omega t$

The current through the load resistor R_L is give By

$I_1 = I_m \sin\omega t$ for $0 \le \omega t \le \pi$

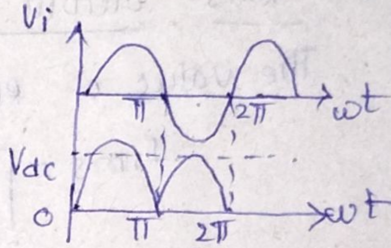
$I_1 = 0$ for $\pi \le \omega t \le 2\pi$

Similarly the current through Diode D_2 and load Resistor R_L is given by

$I_2 = 0$ for $0 \le \omega t \le \pi$

$I_2 = I_m \sin\omega t$ for $\pi \le \omega t \le 2\pi$

$\therefore$ The total current $I = I_1 + I_2$



Average (or) DC out put current :⇒

Idc is given by

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_1\, d(\omega t) + \frac{1}{2\pi}\int_{\pi}^{2\pi} I_2\, d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin\omega t\, d(\omega t) + 0 + \int_{\pi}^{2\pi} I_m \sin\omega t\, d\omega t\right]$$

$$= \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi} = 0.318\, I_m$$

$$\therefore I_{dc} = \frac{2I_m}{\pi}$$

Substituting the value of I_m

$$I_m = \frac{V_m}{R_f + R_L}$$

$$I_{dc} = \frac{2}{\pi}\frac{V}{(R_f + R_L)}$$

R_f is the forward Dynamic Resistance of the diode.

(ii) Average (or) DC output voltage (V_{ac} or V_{dc})

The dc output voltage is given by

$$V_{dc} = I_{dc} \times R_L = \frac{2I_m}{\pi} \times R_L$$

$$V_{dc} = \frac{2}{\pi} \frac{V_m R_L}{R_f + R_L}$$

If $R_L >> R_f$ then $V_{dc} = \frac{2V_m}{\pi}$

iii) RMS output current:→

The value of RMS current is given by

$$I_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} I_L^2 \, d(\omega t)\right]^{1/2}$$

$$= \frac{1}{2\pi}\int_0^{\pi} I_1^2 d(\omega t) + \frac{1}{2\pi}\int_{\pi}^{2\pi} I_2^2 d(\omega t)\Big]^{1/2}$$

$$= \left[\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\omega t \, d(\omega t) + \frac{1}{2\pi}\int_{\pi}^{2\pi} I_m^2 \sin^2\omega t \, d(\omega t)\right]^{1/2}$$

$$= \frac{I_m^2}{2\pi}\int_0^{\pi}\left[\frac{1-\cos 2\omega t}{2}\right]d(\omega t) + \frac{I_m^2}{2\pi}\int_{\pi}^{2\pi}\left[\frac{1-\cos 2\omega t}{2}\right]d(\omega t)\Big]^{1/2}$$

$$= \left[\frac{I_m^2}{4\pi}\left[\omega t - \frac{\sin 2\omega t}{\omega t}\right]_0^{\pi} + \frac{I_m^2}{4\pi}\left[\omega t - \frac{\sin 2\omega t}{\omega t}\right]_{\pi}^{2\pi}\right]^{1/2}$$

$$= \left[\frac{I_m^2}{4\pi}(\pi - 0) - 0\right] + \frac{I_m^2}{4\pi}(2\pi - 0) - (\pi - 0)\Big]^{1/2}$$

$$= \left[\frac{I_m^2}{4\pi} \times \pi \times \frac{I_m^2}{4\pi} \times \pi\right]^{1/2} = \left(2 \times \frac{I_m^2}{4}\right)^{1/2} = \frac{I_m}{\sqrt{2}}$$

$$\therefore I_{rms} = \frac{I_m}{\sqrt{2}}$$

iv) RMS output voltage: (V_{rms}):→

RMS voltage across the load is given by

$$V_{rms} = I_{rms} \times R_L = \frac{V_m}{\sqrt{2}(R_f + R_L)} \times R_L$$

$$V_{rms} = \frac{V_m}{\sqrt{2}\left(1 + \frac{R_f}{R_L}\right)}$$

if $R_L >> R_f$ them $V_{rms} = \frac{V_m}{\sqrt{2}}$

v) <u>Rectifier Efficiency</u> :⇒

The ratio of DC output power to the ac input power

$$\therefore \eta = \frac{P_{dc}}{P_{ac}}$$

$$P_{dc} = I_{dc}^2 \times R_L = \frac{4 I_m^2 R_L}{\pi^2}$$

$$P_{ac} = I_{rms}^2 (R_L + R_f)$$

$$\% = \frac{P_{ac}}{P_{dc}} = \frac{4 I_m^2 R_L}{\pi^2} \times \frac{2}{I_m^2 (R_L + R_f)}$$

$$\% \eta = \frac{81.2}{1 + \frac{R_f}{R_L}}$$

∴ Theoritically rectifier efficiency is 81.2%. when $\frac{R_L}{R_f} = 0$.

<u>Ripple factor</u>:⇒

It is given by $\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$ (or) $\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$

$$\gamma = \sqrt{\left[\frac{I_m}{\sqrt{2}} \times \frac{\pi}{2 I_m}\right]^2 - 1}$$

$$\gamma = \sqrt{\left[\frac{\pi}{2\sqrt{2}}\right]^2 - 1} = 0.48 \Rightarrow \gamma = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = 0.48.$$

<u>% of Regulation</u>:⇒ $\frac{V_{no\,load} - V_{Full\,Load}}{V_{Full\,load}}$

$$= \frac{\frac{2V_m}{\pi} - \left[\frac{2V_m}{\pi} - I_{dc} R_f\right]}{\frac{2V_m}{\pi} - I_{dc} R_f} \times 100$$

$$= \frac{I_{dc} R_f}{I_{dc} R_L} \times 100$$

$$\% \text{ Regulation} = \frac{R_f}{R_L} \times 100$$

$\left[\because V_{dc} = I_{dc} \times R_C = \frac{2 I_m R_L}{\pi} = \frac{2V_m}{\pi} - I_{dc} R_f\right]$

<u>Transformer utilization factor</u>:⇒

$$\therefore TUF = \frac{(TUF)_P + (TUF)_S + (TUF)_S}{2}$$

$$= \frac{0.812 + 0.287 + 0.287}{2} = 0.693$$

$$(TUF)_{ON} = 0.693$$

Peak Inverse voltage :⇒ It is the maximum possible voltage across diode when it is Reverse biased

$$D_2 = V_m + V_m = 2V_m$$

Form factor :⇒ It is defined as the rms value of the ac component present in the output to the average value of the component present in the dc output

$$F = \frac{\frac{I_m}{\sqrt{2}}}{\frac{2I_m}{\pi}} = \frac{0.707 I_m}{0.63 I_m}$$

$$= 1.12$$

Peak factor :⇒ It is defined as the ratio of peak value of the output to the rms value of the ac component present in the output

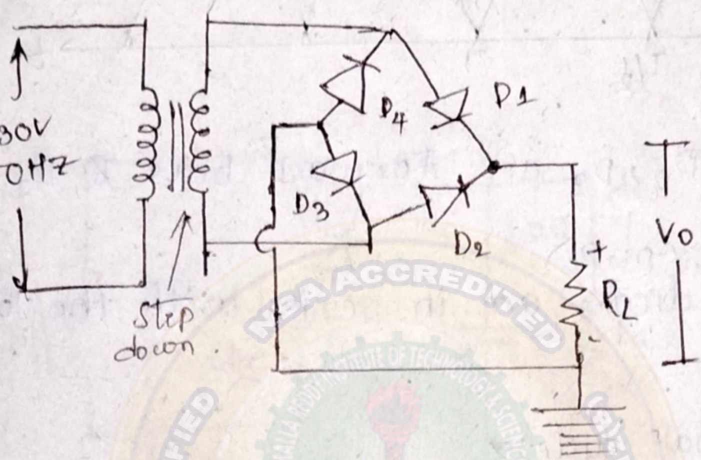
$$P = \frac{I_m}{I_m/\sqrt{2}} = \sqrt{2} = 1.414$$

BRIDGE RECTIFIER :⇒ (Without filter)

→ The full wave rectifier circuit requires a center tapped transformer.

→ In full wave rectifier only one half of the total AC voltage is utilized to convert into DC output.

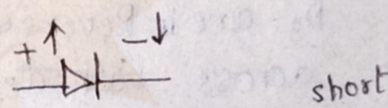
→ The need of centre tapped transformer is eliminated in the bridge rectifier circuit.



CONSTRUCTION :⇒

→ In this Bridge Rectifier circuit one step down transformer and 4 diodes, 1 Load resistor is used. Here the 4 diodes are connected in the form of bridge so it is called Bridge rectifier.

→ The output is taken across the R_L.

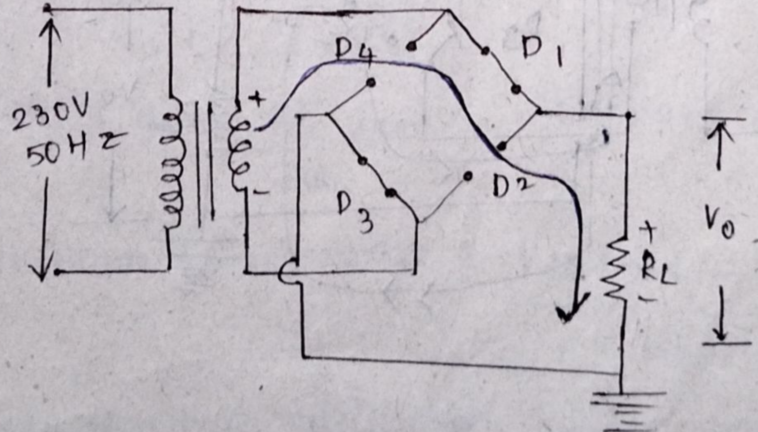


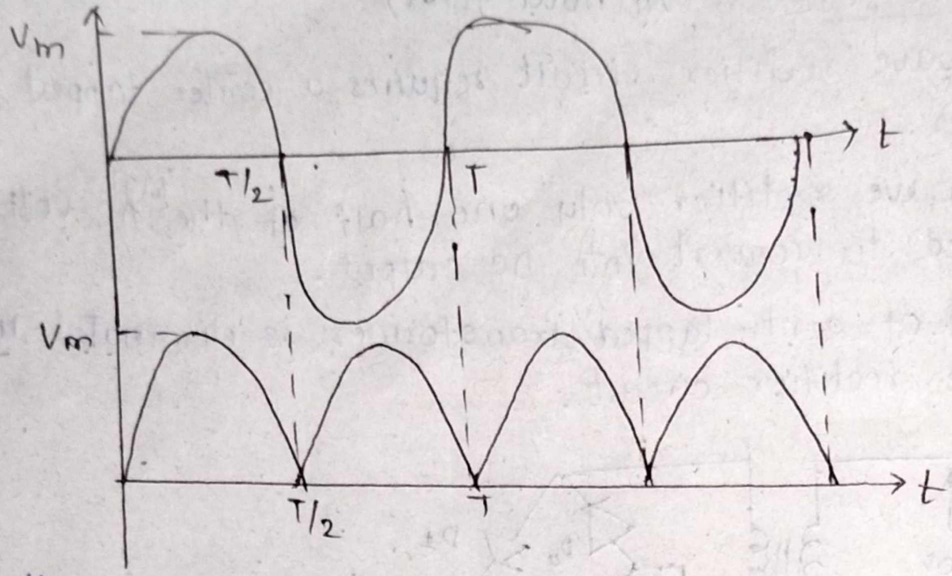
D_1, D_3 Forward bias → ON

D_2, D_4 Reverse bias → OFF → open.

Operation :⇒

During the positive half cycle :⇒



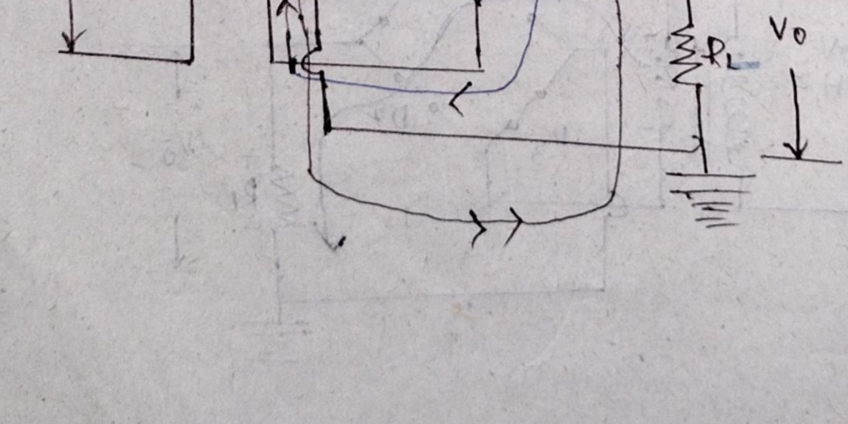


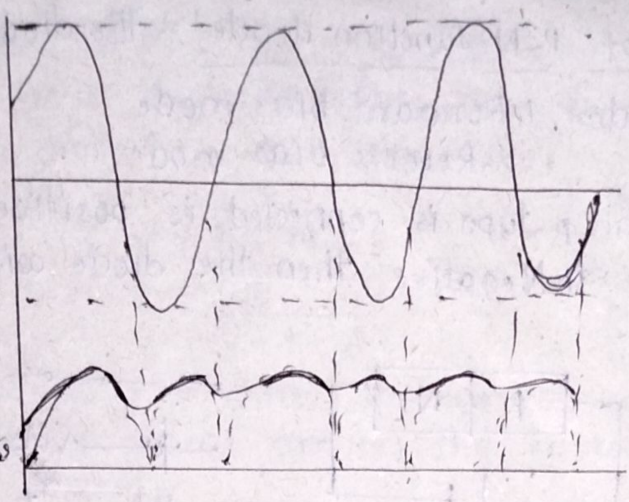
→ In this case D_1, D_3 are Forward bias & D_2, D_4 are reverse bias

→ The conducting diodes (D_1, D_3) are in series with the load resistor R_L

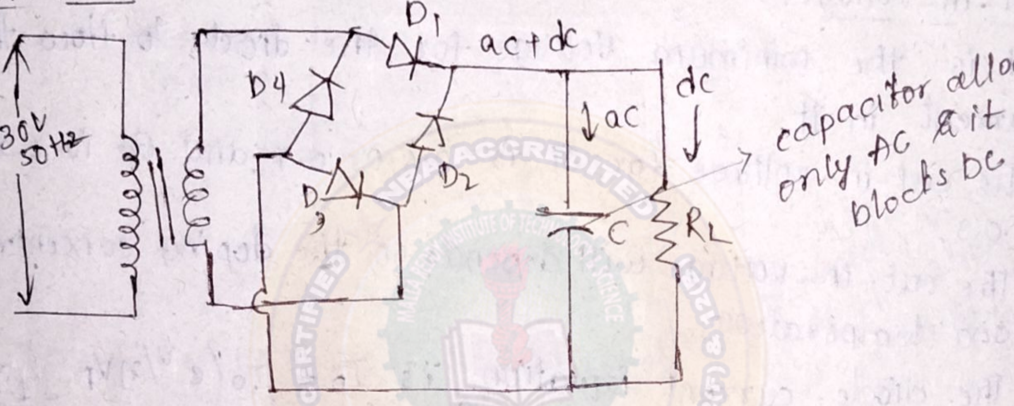
During Negative half cycle :⇒

→ During the -ve half cycle the +ve voltage will deliever across the anodes of D_2 and D_4, the -ve voltage will deliver across the cathodes of D_2 and D_4. So, the diodes D_2 and D_4 are in Forward Bias and the diode D_1 and D_3 are in Reverse Bias because of the +ve power supply across cathode of D_1 and D_3.





With filter



Analysis:→

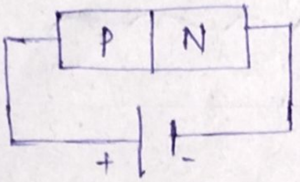
1. DC output current are average current $I_{dc} = \frac{2I_m}{\pi}$
2. average voltage (or) DC output voltage

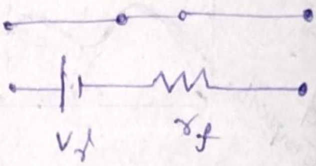
$$V_{dc} = \frac{2V_m}{\pi}$$

3. RMS current = $I_{rms} = \frac{I_m}{\sqrt{2}}$
4. Rms voltage $V_{rms} = \frac{V_m}{\sqrt{2}}$
5. Efficiency $\eta = \frac{P_{dc}}{P_{ac}} \times 100$. fullwave rectifier = 81.2%
6. percentage of regulation = $\frac{V_{No\,Load} - V_{Full\,Load}}{V_{FULL\,LOAD}} \times 100$
7. Transformer utilisation factor TUF = 0.693
8. Form factor = 1.12
9. Peak factor = $\sqrt{2}$ = 1.414 . * ripple factor = 0.482

V-I characteristics of P-N Junction diode :⇒ The diode will operated in 2 modes 1. Forward bias mode
2. Reverse bias mode.

Forward Bias :⇒ The p-type is connected is positive and N-type is connected to Negative then the diode will be in forward Bias.





Cut-in-voltage :⇒

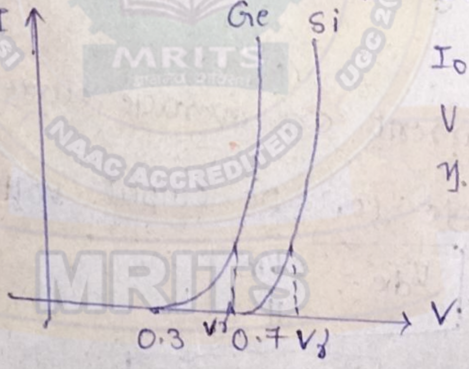
→ It is the minimum voltage for the diode to flow the current in it.

→ The cut-in-voltage for Si is 0.6 or 0.7 and Ge is 0.2 (or) 0.3.

→ The cut-in-voltage will depends on the doping concentration and temperature.

→ The diode current Equation is $I_D = I_0(e^{V/\eta V_T} - 1)$

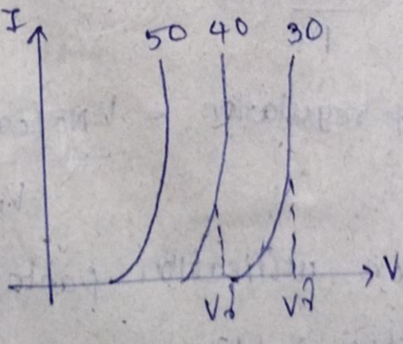
I_0 Leakage current
V - Junction voltage
η -



$$I_D = I_0 e^{V/\eta V_T} - I_0$$

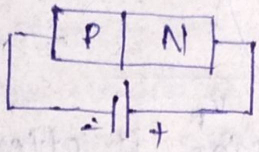
$$I_D = I_0 e^{V/\eta V_T} \quad [\because I_0 << I_0 e^{V/\eta V_T}]$$

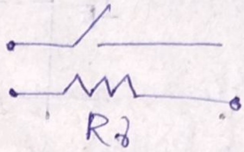
→ If increase in the temperature the cut-in-voltage will decrease.



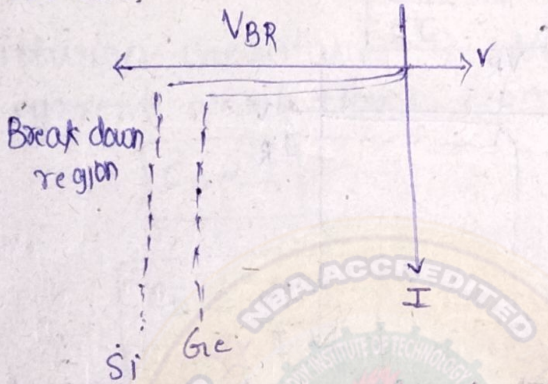
Reverse bias condition :⇒

The p-type is connected into -ve & n-type is connected to +ve then the diode is in reverse bias.





→ In Reverse bias condition the current will flow because of minority charge carriers that current is called as Leakage current.



$I_D = I_0(e^{V/\eta V_T} - 1)$ (Negative :⇒ It is not -ve current only direction is opposite).

$I_D = I_0 e^{V/\eta V_T} - I_0$

$I_D = -I_0$ $[\because I_0 >> I_0 e^{V/\eta V_T}]$

Diode Static Resistance :⇒

→ The diode offers 2 resistance

1. Static Resistance.
2. Dynamic Resistance.

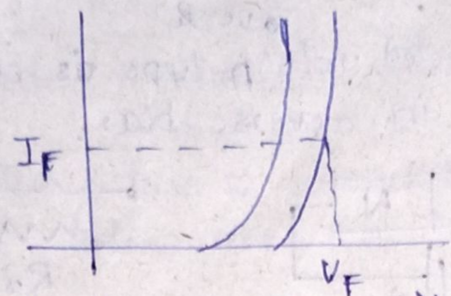
1. **Static Resistance :⇒** It is the resistance offered by the p-n junction diode under DC conditions. Therefore the static resistance is also called as DC resistance.

→ It is the ratio of voltage across the diode to current through the diode.

$$\boxed{R_s = \frac{V_D}{I_D}}$$

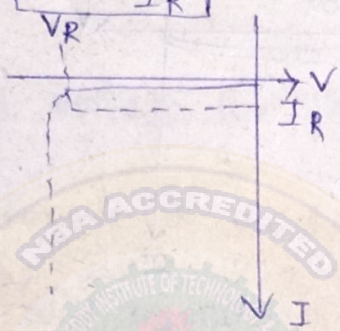
→ The resistor offered in forward bias condition is called forward static resistance.

$$\boxed{R = \frac{V_F}{I_F}}$$



→ When diode is in Reverse bias it offers some resistance that resistance is reverse static resistance.

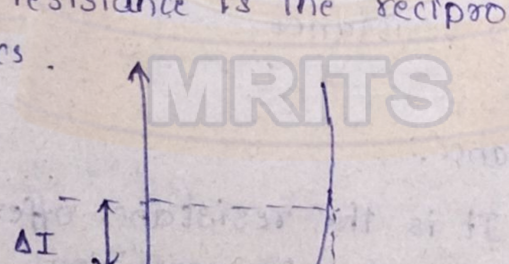
$$R = \frac{V_R}{I_R}$$



Dynamic Resistance :→ It is the resistance offered by the p-n junction diode under AC conditions. Therefore the dynamic resistance is also called as AC resistance.

→ The DC resistance is always greater than Dynamic resistance the dynamic resistance is represented with 'r'.

→ The Dynamic resistance is the reciprocal of the V-I characteristics.



$$r = \frac{1}{\text{slope}}$$

$$= \frac{1}{\Delta I / \Delta V} = \boxed{r = \frac{\Delta V}{\Delta I}}$$

$$\boxed{r = \frac{\eta V_T}{I}}$$

Forward dynamic Resistance :⇒ $r_F = \frac{\eta V_T}{I_F}$

Diffusion Capacitance :⇒

→ change in the charge with respect to change in voltage is called capacitance.

→ In Forward Bias condition the p-n junction diode offers some capacitance that capacitance is called Diffusion capacitance.

→ Generally it ranges from nano faraday (10^{-9}) to Micro Farad
nF − μF

→ The diffusion capacitance is directly proportional to the current which flows from the junction.

$$C_D \propto I$$

∴

$$C_D = \frac{\tau \cdot I}{\eta V_T}$$

→ The diffusion capacitance is possible due to the holes & due to the electrons.

Diode Switching Characteristics :⇒

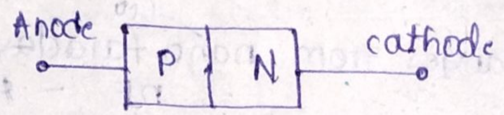
1. Switching time of a P-N Junction diode is depends on Reverse recovering time.
2. For fast switching operations the reverse recovering time should be less.
3. Switching time of a pn junction diode is 9-10 times of Reverse recovering time.
4. Commerically the available P-N Junction diodes are with the switching speed of micro seconds - Nano seconds, where as specially designed P-N Junction diodes gives the switching speed of range pico seconds. (10^{-12})

Zener diode :→

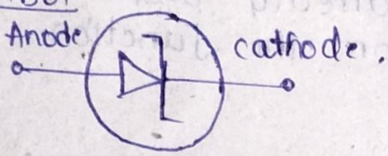
→ A diode which is designed with power dissapation capabilities and to operate in break down region.

→ The zener diode is a heavily doped P-N Junction diode

→ To make the zener diode silicon is used because it with stands for higher temperature.

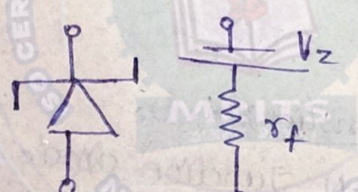


Symbol



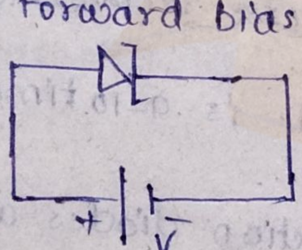
→ The zener diode forward characteristics are similar to the Normal PN Junction diode but the cut-in voltage is greater than the P-N Junction diode.

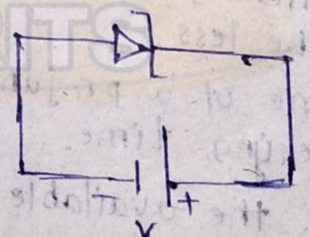
→ The zener diode always operates in reverse breakdown region.



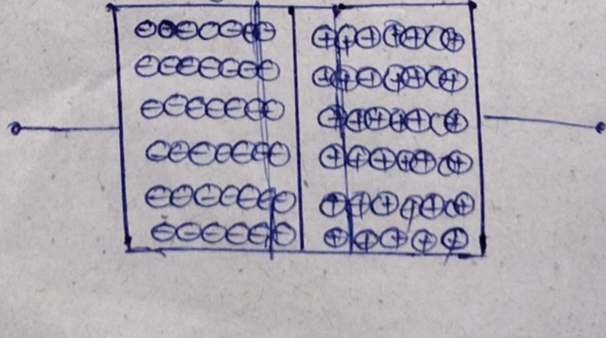
→ The zener diode will operate in 2 modes

1. Forward bias
2. Reverse bias.





→ The Zener diode breakdown occurs, ~~in~~ because of Avalanche Effect i.e Avalanche Break down, Zener Break down



Reverse Bias:→ Condition:→

→ The zener diode is designed to operate in Reverse bias mode i.e it going to be work in reverse break down region.

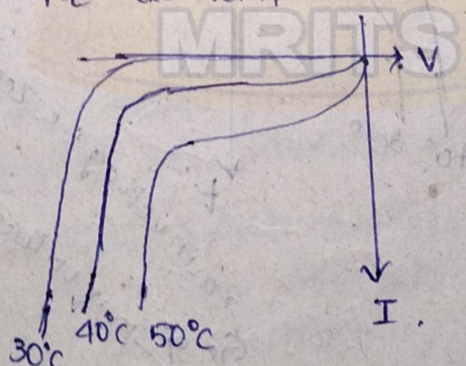
→ AT Low doping concentration at high reverse bias Avalanche Break down occurs.

→ AT high doping concentration and Low reverse bias zener Break down occurs.

→ Initially available charge carriers do not acquire sufficient energy to distrubt the bond. But it is possible to initiate break down through direct rapture of the bond because of existence of strong electric field across the junction.

→ The zener breakdown happens at less than 6volts.

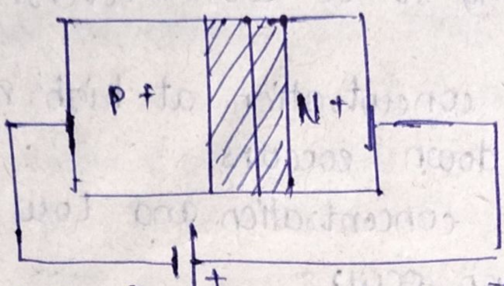
→ zener break down voltage is having negative temperature co-efficient i.e as temperature ↑ breakdown voltage ↓.



→ The zener breakdown voltage is less than the Avalanche breakdown voltage.

Avalanche Break down:⇒

p – moderately doped
p+ – heavily doped
p++ → degenerated & heavily doped



→ Avalanche Breakdown occurs at greater than 6 volts.

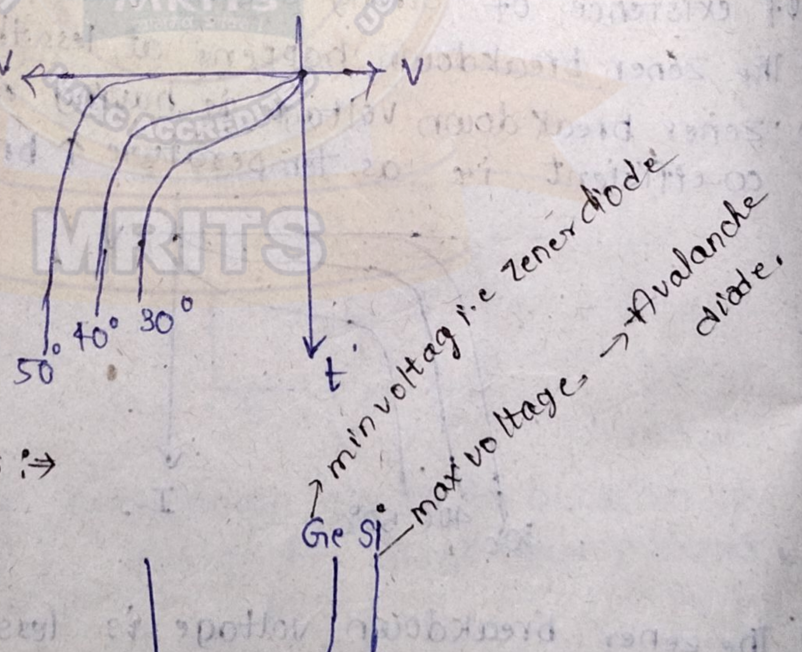
→ Thermally generated electrons and holes acquries sufficient energy from the applied potential to produce new carriers by removing valency electrons from their bonds.

→ This new carrier produce additional carrier by disturbing the bonds.

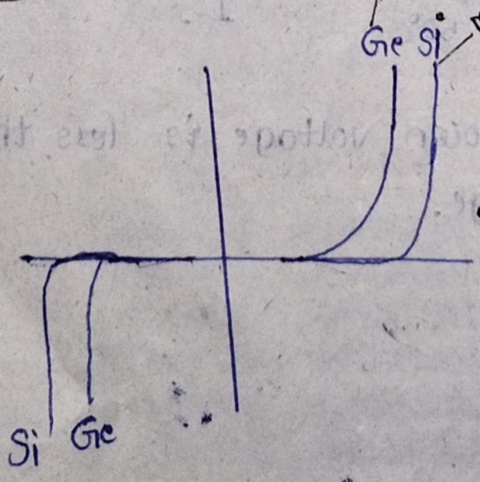
→ This cumulative process is called Avalanche effect.

→ If breakdown occurs due to avalanche effect then it is called Avalanche break down.

→ Avalanche Breakdown voltage is having +ve temperature cofficient i.e temperature ↑ breakdown voltage also ↑

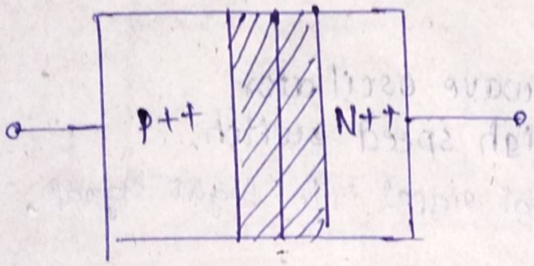


V-I characteristics :⇒

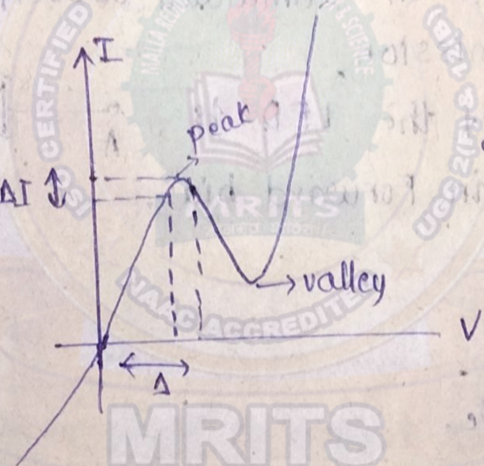


Tunnel Wave/diode :→

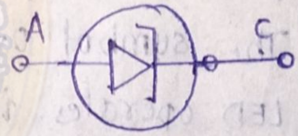
1. It is a special type P-N Junction diode.
2. It is made up of degenerative semi conductor



3. In Tunnel diode the cut-in-voltage more than normal P-N Junction diode.
4. In Tunnel diode the depletion region width is around 100 A°.
5. The V-I characteristics of a Tunnel diode is shown below:



symbol



→ The peak and valley points of Tunnel diode offers 0' conductivity and infinite resistance.

→ In Between these points the tunnel diode offers -ve' resistance and these characteristics is used to degenerate into oscillations.

Advantages :→

1. Low cost.
2. small size.
3. Low noise.
4. low power
5. Simple to Fabricate.

Disadvantage:⇒

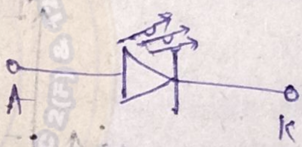
1. It is 2-terminal device.
2. Low output swing.

Applications:⇒

1. It used as Microwave oscillator
2. It is used as high speed switch.

LED:⇒ Converts electrical signal into Light signal.

→ LED stands for Light emitting diode.
→ LED is also like Normal PN-Junction diode, but its doping concentration is slightly more than the normal PN Junction diode.
→ LED made up of direct band gap semiconductors.
→ LED works based on stimulated absorption and spontaneous emission.
→ The symbol of the LED is



→ LED operates in Forward bias.

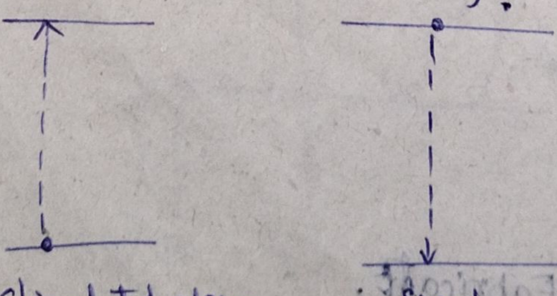
Advantages:⇒

1. Low cost
2. Simple Fabricate.
3. Simple drive circuit.
4. Low temperature dependency.

Disadvantages:⇒

1. Low directivity
2. Harmonic distortion.
3. Low coupling power efficiency.

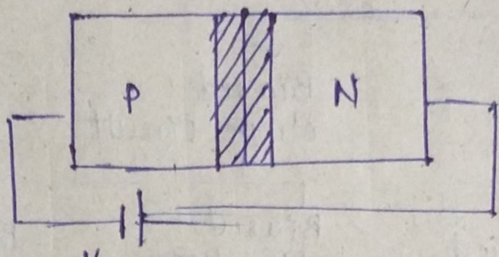
Electrical = Light



Stimulated atom   Spontaneous Emission.

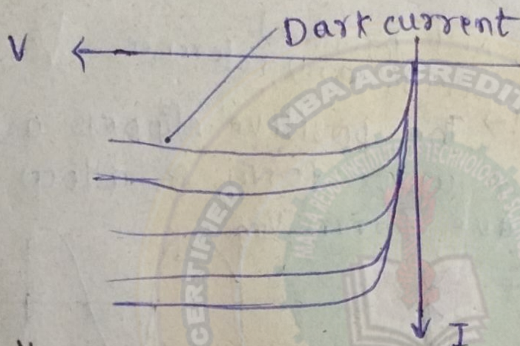
photo diode :→ convert light signal into electrical signal.

It is also like Normal PN Junction diode. But its doping concentration is slightly less than the Normal PN Junction Diode.



→ photo diode operates In Reverse Bias

The (element) current is $I_P = I_0 \left[1 - e^{-V/nV_T}\right] + I_s$

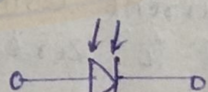


light = Electrical

Respensivity :→ It is the ratio of photo diode output current to incident power;

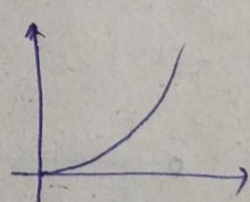
$$R = \frac{I_P}{P_0} \text{ A/W}$$

"The photo diode is used to convert the light signal into electrical signal".

→ The symbol of photo diode is 

Advantages :→

1. Simple and Fabricate
2. Low cost
3. Linearity
4. Low Temperature Dependency.



V-I characteristics.

Dis advantages :→

1. Low coupling power efficiency
2. Harmonic Distribution
3. Low Directivity

CLIPPERS: ⇒ The clipper circuits are used to avoid the unwanted portion of the wave form.

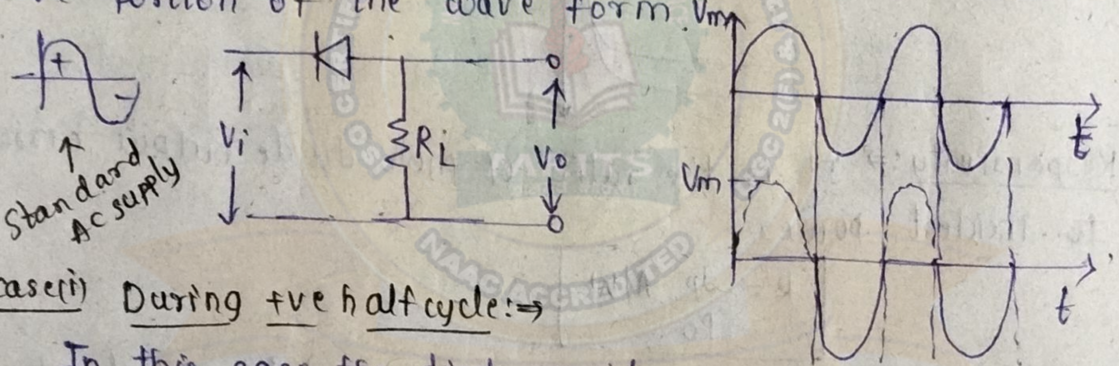
→ It is also called as limiters, slicers, Amplitude selectors.

Types of clippers.

- UnBiased Clipper circuit
  - unbiased +ve clipper
    - Unbiased series +ve clipper
    - Unbiased series -ve clipper
  - Unbiased -ve clipper
    - series
    - shunt
- Biased clipper Circuit
  - Biased +ve clipper
    - series
    - shunt.
  - Biased -ve clipper
    - series
    - shunt

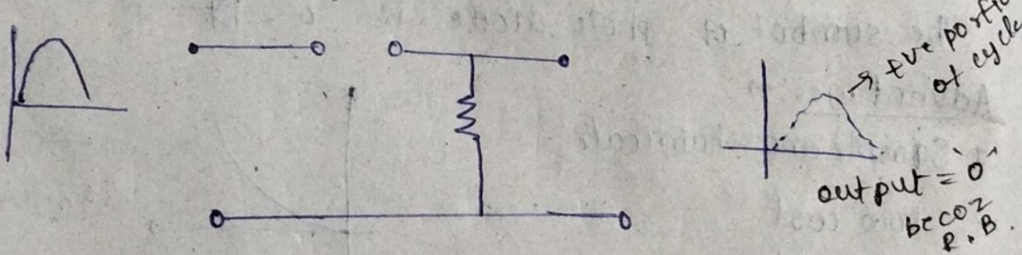
(UnBiased) → does not provided with any reference.

UnBiased Positive clipper: → The positive clippers are used to clip the +ve portions of wave form & allow the -ve portion of the wave form.

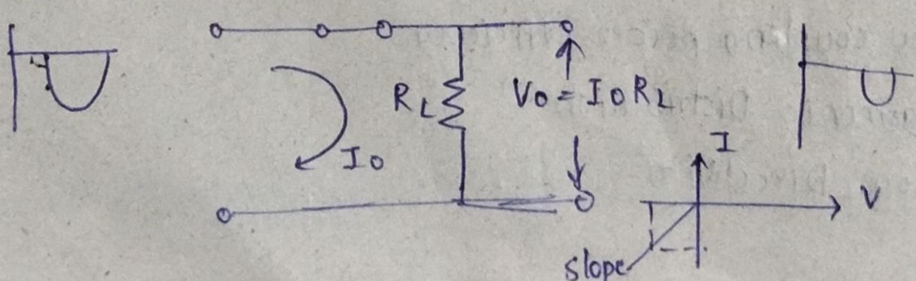


case(i) During +ve half cycle: ⇒

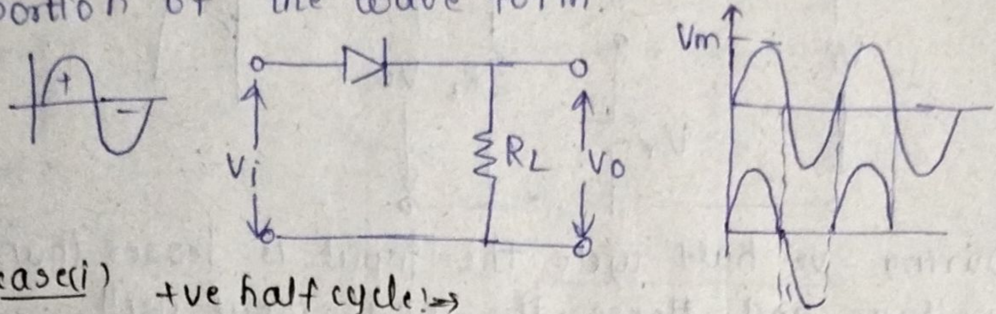
In this case the diode consider Reverse Bias i.e open circuit, no current will flow through R_L and Hence out put is equal to zero.



case ii During -ve half cycle: → In this case consider F.B i.e short circuit & Hence the total current will Relivered across R_L

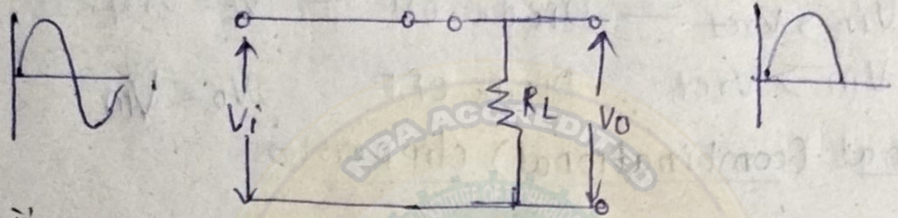


Un-Biased -ve clipper :→ The -ve clippers are used to clip the -ve portions of the wave form and allow the +ve portion of the wave form.

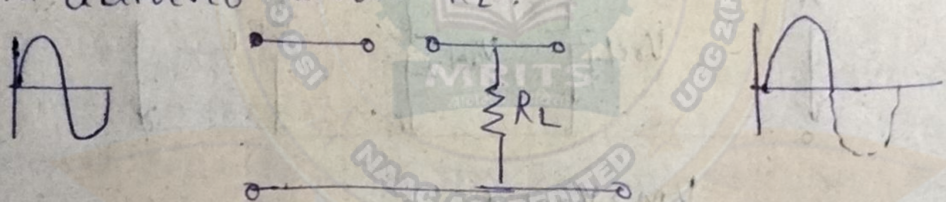


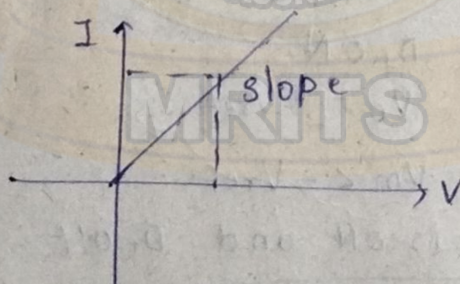
case(i) +ve half cycle:→

In this case the diode D is in forward bias condition i.e "ON state" and hence the total current will delivered across the RL

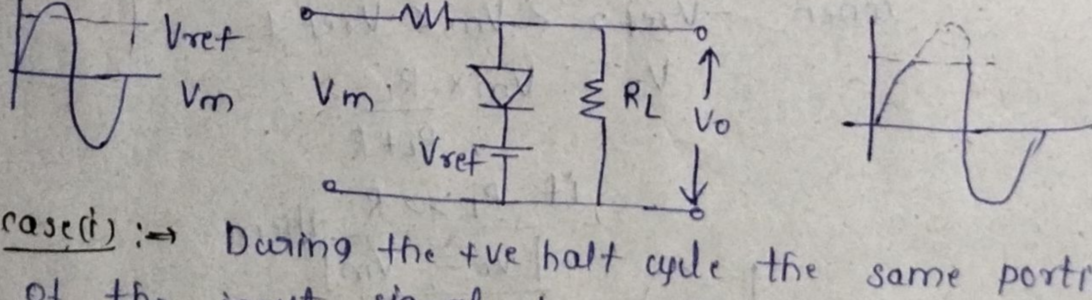


case ii -ve half cycle:→ In this case the diode D is in Reverse bias i.e "off state" and hence no current will delivered across RL.

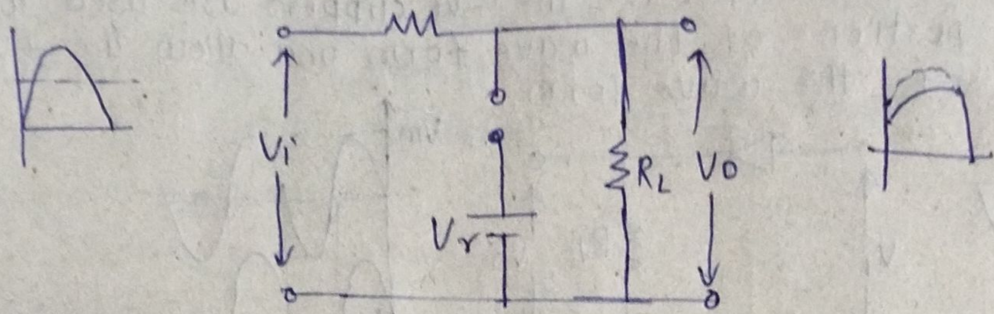




+ve Biased clipper:→



case(i) :→ During the +ve half cycle the same portion of the input signal lesser than reference voltage. In this case the diode is In R.B i.e S.C. and Hence the total current will developed across RL



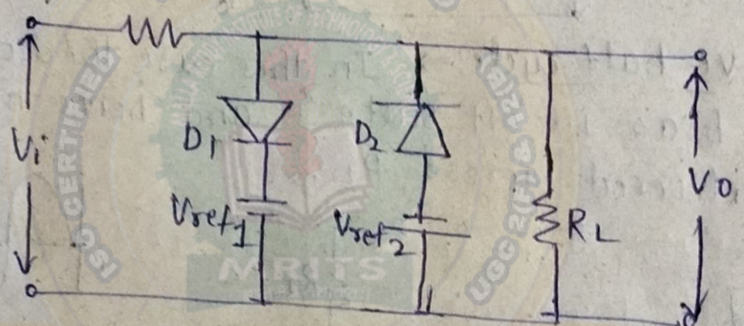
case ii During −ve half cycle the input is lesser than Reverse voltage and Hence the total input will delivered across the R_L.

→ The input above the reference voltage will be left

$V_{in} > V_{ref}$ — Diode ON — $V_O = V_{ref}$

$V_{in} > V_{ref}$ Diode OFF $V_O = V_m$

Bidirectional (combinational) clippers :→



when $V_m > V_{ref\,1}$

D_1 ON

$V_O = +V_{ref}$

when $V_m < -V_{ref}$

⇒ Diode D_2 is ON and D_1 off

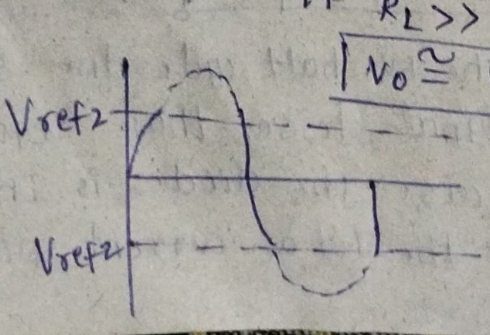
$$\boxed{V_O = -V_{ref}}$$

when $-V_{ref\,2} < V_m < V_{ref\,1}$

$$V_O = V_m \times \frac{R_L}{R_L + R}$$

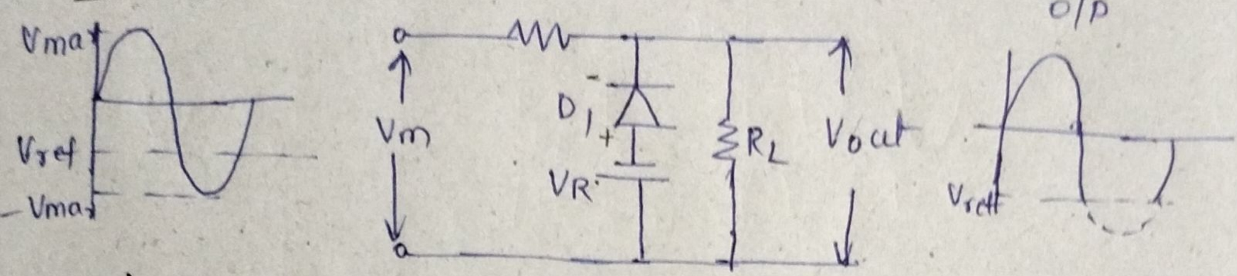
if $R_L >> R$ then

$$\boxed{V_O \simeq V_m}$$



Biased clippers:→ provided with some reference

-ve Biased clippeds:⇒



case(i) During the +ve half cycle the Input voltage is greater than the -ve reference voltage.

→ In this case the diode D_1 is In R.B i.e open circuit & hence the total current will delievered across the R_L Hence **o/p = In/p**

$$V_o = V_m \times \frac{R_L}{R_i + R_L}$$

$$\boxed{V_{max} = V_{max} \cdot \frac{R_L}{R_i + R_L}}$$

case ii ⇒ During the -ve half cycle the Input is less than the -ve reference then the diode is 'ON' state i.e Forward Bias & hence the output voltage Now become

$$\boxed{V_o = -V_{ref}}$$

UNIT-II

BIPOLAR JUNCTION TRANSISTOR

The transistor was invented in 1947 by John Bardeen, Walter Brattain and William Shockley at Bell Laboratory in America.

A transistor is a semiconductor device, commonly used as an Amplifier or an electrically Controlled Switch.

There are two types of transistors:

1) Unipolar Junction Transistor
2) Bipolar Junction Transistor

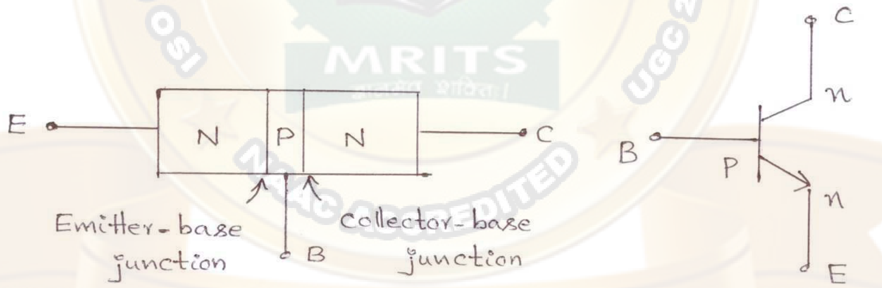
In Unipolar transistor, the current conduction is only due to one type of carriers i.e., majority charge carriers. The current conduction in bipolar transistor is because of both the types of charge carriers i.e., holes and electrons. Hence it is called as Bipolar Junction Transistor and it is referred to as BJT.

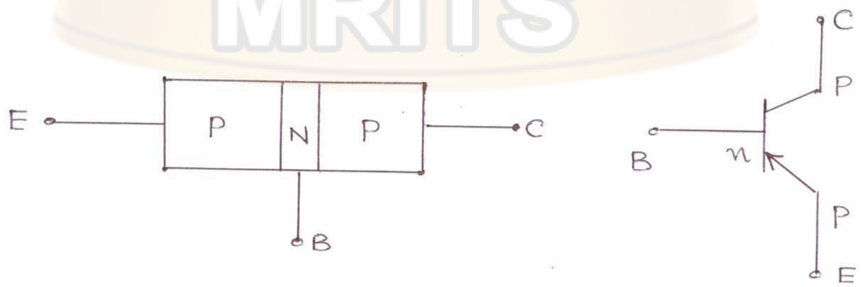
BJT is a semiconductor device in which one type of semiconductor material is sand witched between two opposite types of semiconductor i.e., an n-type semiconductor is sandwiched between two p-type semiconductors or a p-type semiconductor is sandwiched between two n-type semiconductor. Hence the BJTs are of two types.

They are:

1) n-p-n Transistor
2) p-n-p Transistor

The two types of BJTs are shown in the figure below.





The arrow head represents the conventional current direction from p to n.

Transistor has three terminals.

1) Emitter
2) Base
3) Collector

Transistor has two p-n junctions. They are:

1) Emitter-Base Junction
2) Collector-Base Junction

Emitter: Emitter is heavily doped because it is to emit the charge carriers.

Base: The charge carriers emitted by the emitter should reach collector passing through the base. Hence base should be very thin and to avoid recombination, and to provide more collector current base is lightly doped.

Collector: Collector has to collect the most of charge carriers emitted by the emitter. Hence the area of cross section of collector is more compared to emitter and it is moderately doped.

Transistor can be operated in three regions.

1) Active region.
2) Saturation region.
3) Cut-Off region.

Active Region: For the transistor to operate in active region base to emitter junction is forward biased and collector to base junction is reverse biased.

Saturation Region: Transistor to be operated in saturation region if both the junctions i.e., collector to base junction and base to emitter junction are forward biased.

Cut-Off Region: For the transistor to operate in cut-off region both the junctions i.e., base to emitter junction and collector to base junction are reverse biased.

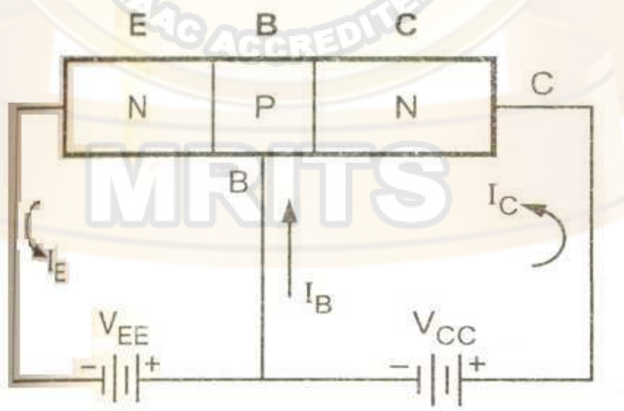
Transistor can be used as

1) Amplifier 2) Switch

For the transistor to act as an amplifier, it should be operated in active region. For the transistor to act as a switch, it should be operated in saturation region for ON state, and cut-off region for OFF state.

Transistor Operation:

Working of a n-p-n transistor:



The n-p-n transistor with base to emitter junction forward biased and collector base junction reverse biased is as shown in figure.

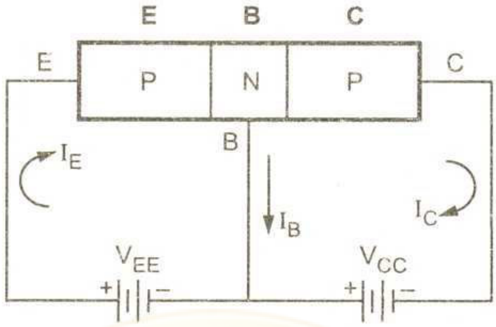
As the base to emitter junction is forward biased the majority carriers emitted by the n-type emitter i.e., electrons have a tendency to flow towards the base which constitutes the emitter current I_E.

As the base is p-type there is chance of recombination of electrons emitted by the emitter with the holes in the p-type base. But as the base is very thin and lightly doped only few electrons emitted by the n-type emitter less than 5% combines with the holes in the p-type base, the remaining more than 95% electrons emitted by the n-type emitter cross over into the collector region constitute the collector current.

The current distributions are as shown in fig

$$\mathbf{I_E = I_B + I_C}$$

Working of a p-n-p transistor:



The p-n-p transistor with base to emitter junction is forward biased and collector to base junction reverse biased is as show in figure.

As the base to emitter junction is forward biased the majority carriers emitted by the p-type emitter i.e., holes have a tendency to flow towards the base which constitutes the emitter current $I_{E.}$

As the base is n-type there is a chance of recombination of holes emitted by the emitter with the electrons in the n-type base. But as the base us very thin and lightly doped only few electrons less than 5% combine with the holes emitted by the p-type emitter, the remaining 95% charge carriers cross over into the collector region to constitute the collector current.

The current distributions are shown in figure.

$$\mathbf{I_E = I_B + I_C}$$

Current components in a transistor:

The figure below shows the various current components which flow across the forward-biased emitter junction and reverse-biased collector junction in P-N-P transistor.

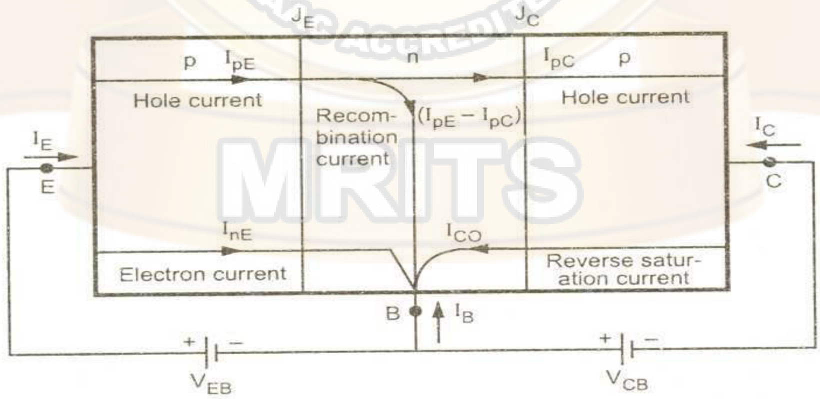


Figure. Current components in a transistor with forward-biased emitter and reverse-biased collector junctions.

The emitter current consists of the following two parts:

1) Hole current I_{pE} constituted by holes (holes crossing from emitter into base).
2) Electron current I_{nE} constituted by electrons (electrons crossing from base into the emitter).

Therefore, Total emitter current $I_E = I_{pE}$ (majority)**+** I_{nE} (Minority)

The holes crossing the emitter base junction J_E and reaching the collector base junction J_C constitutes collector current I_{pC}.

Not all the holes crossing the emitter base junction J_E reach collector base junction J_C because some of them combine with the electrons in the n-type base.

Since base width is very small, most of the holes cross the collector base junction J_C and very few recombine, constituting the base current ($I_{pE} - I_{pC}$).

When the emitter is open-circuited, I_E=0, and hence I_{pC}=0. Under this condition, the base and collector together current I_C equals the reverse saturation current I_{CO}, which consists of the following two parts: I_{PCO} caused by holes moving across I_C from N-region to P-region.

I_{nCO} caused by electrons moving across I_C from P-region to N-region. $I_{CO} = I_{nCO} + I_{pCO}$

In general, $I_C = I_{nC} + I_{pC}$

Thus for a P-N-P transistor, $\mathbf{I_E = I_B + I_C}$

Transistor circuit configurations:

Following are the three types of transistor circuit configurations:

1) Common-Base (CB)
2) Common-Emitter (CE)
3) Common-Collector (CC)

Here the term 'Common' is used to denote the transistor lead which is common to the input and output circuits. The common terminal is generally grounded.

It should be remembered that regardless the circuit configuration, the emitter is always forward-biased while the collector is always reverse-biased.

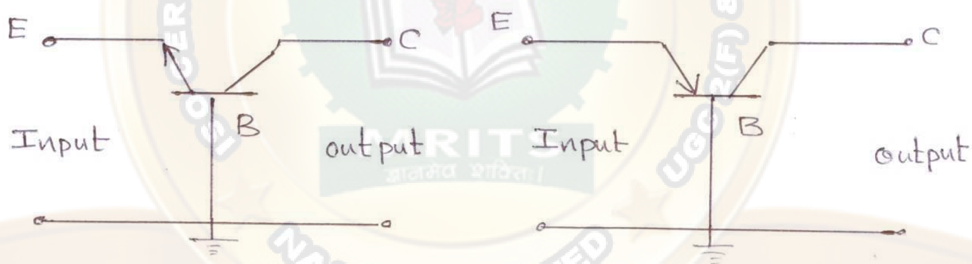


Fig. Common – Base configuration

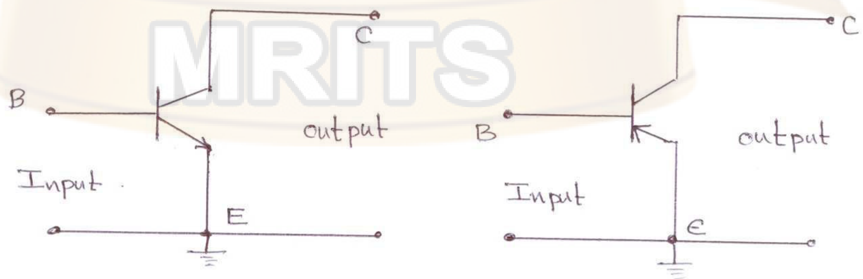


Fig. Common – emitter configuration

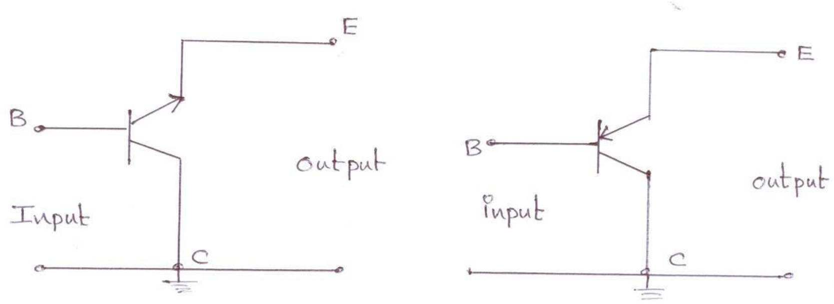


Fig. Common – Collector configuration

Common – Base (CB) configurations:

In this configuration, the input signal is applied between emitter and base while the output is taken from collector and base. As base is common to input and output circuits, hence the name common-base configuration. Figure show the common-base P-N-P transistor circuit.

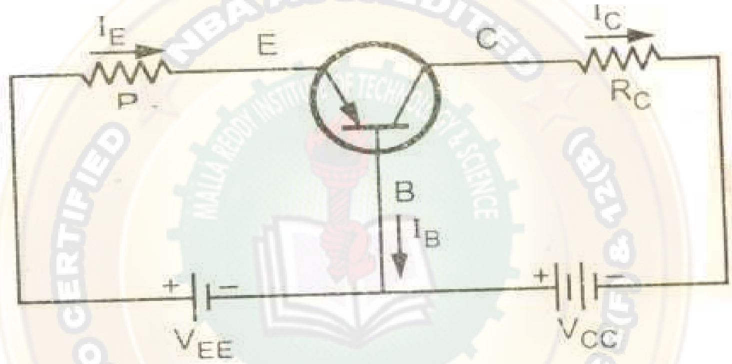


Fig. Common – base PNP transistor amplifier.

Current Amplification Factor (α) :

When no signal is applied, then the ratio of the collector current to the emitter current is called dc alpha (α_{dc}) of a transistor.

$$\alpha_{dc} = \frac{-I_C}{I_E}$$,.............. (1) (Negative sign signifies that I_E flows into transistor while I_C flows out of it).

'α' of a transistor is a measure of the quality of a transistor. Higher is the value of 'α', better is the transistor in the sense that collector current approaches the emitter current.

By considering only magnitudes of the currents, $I_C = \alpha I_E$ and hence $I_B = I_E - I_C$

Therefore, $I_B = I_E - \alpha I_E = I_E(1-\alpha)$ .... (2)

When signal is applied, the ratio of change in collector current to the change in emitter current at constant collector-base voltage is defined as current amplification factor,

$$\alpha_{dc} = -\frac{\Delta I_C}{\Delta I_E}$$ .... (3)

For all practical purposes, $\alpha_{dc} = \alpha_{ac} = \alpha$ and practical values in commercial transistors range from 0.9 to 0.99.

Total Collector Current:

The total collector current consists of the following two parts:

i) αI_E , current due to majority carriers
ii) I_{CBO}, current due to minority carriers

∴ Total collector current $I_C = \alpha I_E + I_{CBO}$ .... (4)

The collector current can also be expressed as $I_C = \alpha (I_B+I_C) + I_{CBO}$ (∵ $I_E = I_B + I_C$)

$$\Rightarrow I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$\Rightarrow I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO} \quad \text{.... (5)}$$

Common-Emitter (CE) configuration:

In this configuration, the input signal is applied between base and emitter and the output is taken from collector and emitter. As emitter is common to input and output circuits, hence the name common emitter configuration.

Figure shows the common-emitter P-N-P transistor circuit.

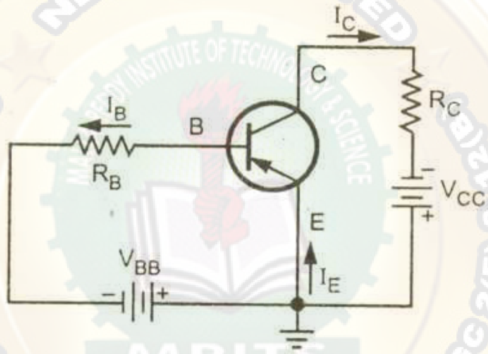


Fig. Common-Emitter PNP transistor amplifier.

Current Amplification Factor (β):

When no signal is applied, then the ratio of collector current to the base current is called dc beta (β_{dc}) of a transistor.

$$\beta_{dc} = \beta = \frac{I_C}{I_B} \quad \text{.................. (1)}$$

When signal is applied, the ratio of change in collector current to the change in base current is defined as base current amplification factor. Thus,

$$\beta_{dc} = \beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{.............(2)}$$

From equation (1), $I_C = \beta I_B$

Almost in all transistors, the base current is less than 5% of the emitter current. Due to this fact, 'β' ranges from 20 to 500. Hence this configuration is frequently used when appreciable current gain as well as voltage gain is required.

Total Collector Current:

The Total collector current $I_C = \beta I_B + I_{CEO}$ .... (3)

Where I_{CEO} is the leakage current.

But, we have, $I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$ ....(4)

Comparing equations (3) and (4), we get

$$\beta = \frac{\alpha}{1-\alpha} \text{ and } I_{CEO} = \frac{1}{1-\alpha} I_{CBO} \quad \text{..........(5)}$$

Relation between α and β:

We know that $\alpha = \frac{I_C}{I_E}$ and $\beta = \frac{I_C}{I_B}$

$I_E = I_B + I_C$ (or) $I_B = I_E - I_C$

Now $$\beta = \frac{I_C}{I_E - I_C} = \frac{\frac{I_C}{I_E}}{1 - \frac{I_C}{I_E}} = \frac{\alpha}{1-\alpha} \quad \text{............... (6)}$$

$$\Rightarrow \beta(1-\alpha) = \alpha \text{ (or) } \beta = \alpha(1+\beta)$$

$$\Rightarrow \alpha = \frac{\beta}{1+\beta} \quad \text{............... (7)}$$

It can be seen that $1 - \alpha = \frac{1}{1+\beta}$ .... (8)

Common – Collector (CC) Configuration:

In this configuration, the input signal is applied between base and collector and the output is taken from the emitter. As collector is common to input and output circuits, hence the name common collector configuration. Figure shows the common collector PNP transistor circuit.

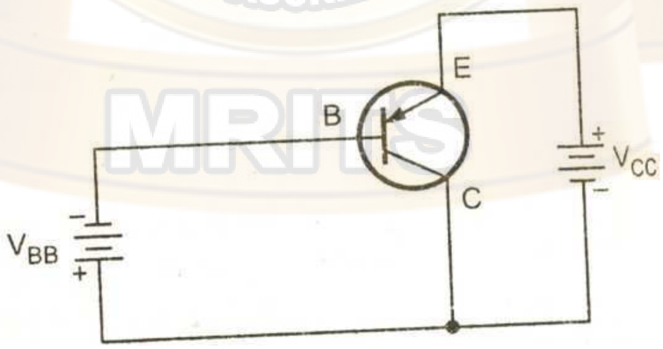


Fig. Common collector PNP transistor amplifier.

Current Amplification Factor (γ):

When no signal is applied, then the ratio of emitter current to the base current is called as dc gamma (γ_{dc}) of the transistor.

$$\gamma_{dc} = \gamma = \frac{I_E}{I_B} \quad \text{.............. (1)}$$

When signal is applied, then the ratio of change in emitter current to the change in base current is known as current amplification factor 'γ'.

$$\gamma_{ac} = \gamma = \frac{\Delta I_E}{\Delta I_B} \qquad \ldots\ldots\ldots\ldots\ldots(2)$$

This configuration provides the same current gain as common emitter circuit as $\Delta I_E \approx \Delta I_C$ but the voltage gain is always less than one.

Total Emitter Current:

We know that $I_E = I_B + I_C$ Also $I_C = \alpha I_E + I_{CBO}$

$$I_E = I_B + (\alpha I_E + I_{CBO})$$

$$\Rightarrow I_E(1-\alpha) = I_B + I_{CBO}$$

$$\Rightarrow I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

(or) $$\Rightarrow I_E = (1+\beta)I_B + (1+\beta)I_{CBO} \qquad \ldots\ldots\ldots\ldots\ldots (3) \qquad \left(\because \frac{1}{1-\alpha} = 1+\beta\right)$$

Relation between γ and α :

We know that $\gamma = \frac{I_E}{I_B}$ and $\alpha = \frac{I_C}{I_B}$

Also $I_B = I_E - I_C$

Now $$\gamma = \frac{I_E}{I_E - I_C} = \frac{1}{1 - \frac{I_C}{I_E}} = \frac{1}{1-\alpha}$$

$$\because \gamma = \frac{1}{1-\alpha} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Relation between γ and β :

We know that $\frac{1}{1-\alpha} = 1+\beta$

$\because$ From equation (4), $$\gamma = \frac{1}{1-\alpha} = 1+\beta \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

Characteristics of Common-Base Circuit:

The circuit diagram for determining the static characteristic curves of an NPN transistor in the common base configuration is shown in fig. below.

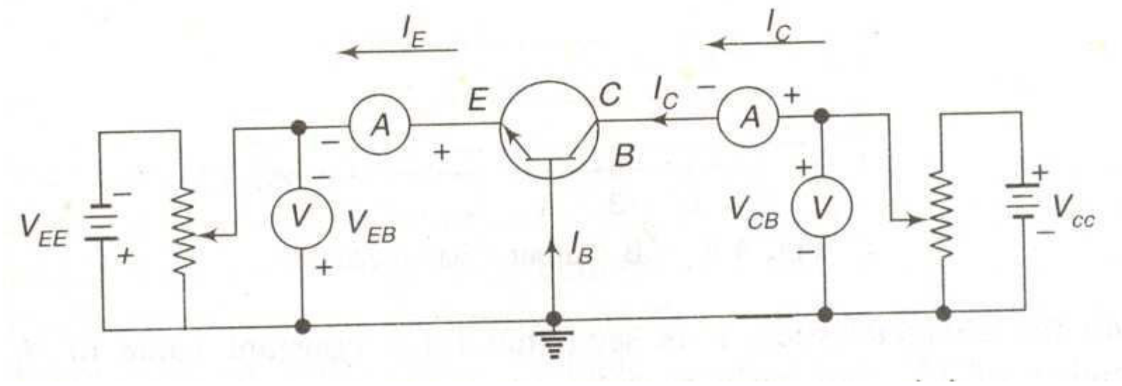


Fig. Circuit to determine CB static characteristics.

Input Characteristics:

To determine the input characteristics, the collector-base voltage V_{CB} is kept constant at zero volts and the emitter current I_E is increased from zero in suitable equal steps by increasing V_{EB}. This is repeated for higher fixed values of V_{CB}. A curve is drawn between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}.

The input characteristics thus obtained are shown in figure below.

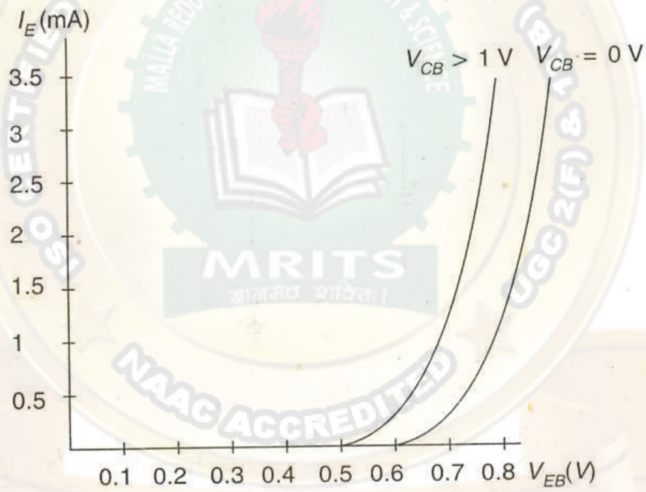
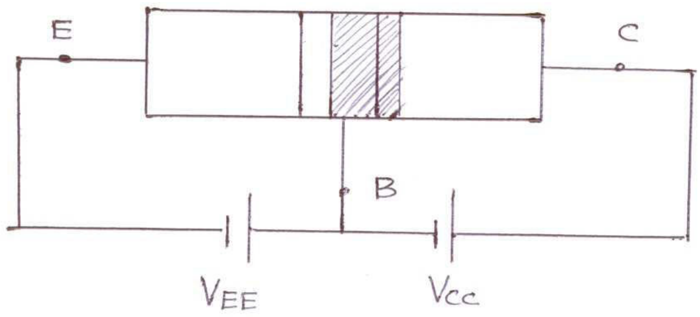


Fig. CB Input characteristics.

Early effect (or) Base – Width modulation:

As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-emitter voltage is known as Early effect (or) Base-Width modulation.



Thus decrease in effective base width has following consequences:

i. Due to Early effect, the base width reduces, there is a less chance of recombination of holes with electrons in base region and hence base current I_B decreases.
ii. As I_B decreases, the collector current I_C increases.
iii. As base width reduces the emitter current I_E increases for small emitter to base voltage.
iv. As collector current increases, common base current gain (α) increases.

Punch Through (or) Reach Through:

When reverse bias voltage increases more, the depletion region moves towards emitter junction and effective base width reduces to zero. This causes breakdown in the transistor. This condition is called "Punch Through" condition.

Output Characteristics:

To determine the output characteristics, the emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}. Then V_{CB} is increased in suitable equal steps and the collector current I_C is noted for each value of I_E. Now the curves of I_C versus V_{CB} are plotted for constant values of I_E and the output characteristics thus obtained is shown in figure below.

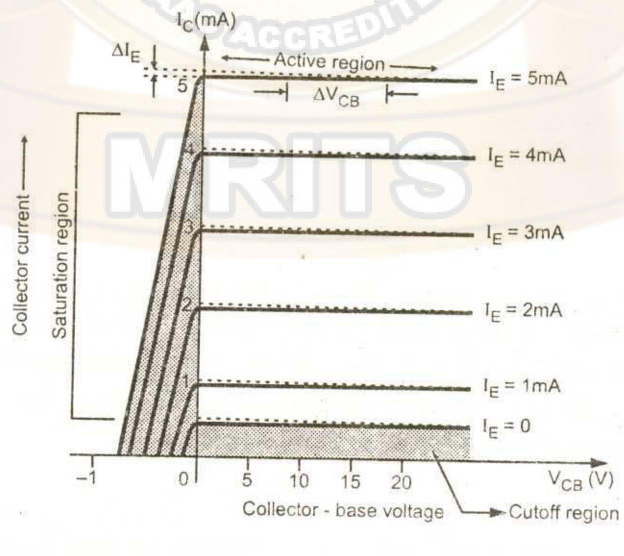


Fig. CB Output characteristics

From the characteristics, it is seen that for a constant value of I_E, I_C is independent of V_{CB} and the curves are parallel to the axis of V_{CB}. Further, I_C flows even when V_{CB} is equal to zero. As the emitter-base junction is forward biased, the majority carriers, i.e., electrons, from the emitter are injected into the base region. Due to the action of the internal potential barrier at the reverse biased collector-base junction, they flow to the collector region and give rise to I_C even when V_{CB} is equal to zero.

Transistor Parameters:

The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common base hybrid parameters (or) h-parameters.

i) Input Impedance (h_{ib}):

It is defined as the ratio of change in (input) emitter to base voltage to the change in (input) emitter current with the (output) collector to base voltage kept constant. Therefore,

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}$$, V_{CB} constant

It is the slope of CB input characteristics curve.

The typical value of h_{ib} ranges from 20Ω to 50Ω.

ii) Output Admittance (h_{ob}):

It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector-base voltage, keeping the (input) emitter current I_E constant. Therefore,

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}$$, I_E constant

It is the slope of CB output characteristics I_C versus V_{CB}.

The typical value of this parameter is of the order of 0.1 to 10μmhos.

iii) Forward Current Gain (h_{fb}):

It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant. Hence,

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}$$, V_{CB} constant

It is the slope of I_C versus I_E curve. Its typical value varies from 0.9 to 1.0.

iv) Reverse Voltage Gain (h_{rb}):

It is defined as a ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current, I_E.

Hence, $$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}$$, I_E constant.

It is the slope of V_{EB} versus V_{CB} curve. Its typical value is of the order of 10^{-5} to 10^{-4}.

Characteristics of Common-Emitter Circuit:

The circuit diagram for determining the static characteristic curves of the an N-P-N transistor in the common emitter configuration is shown in figure below.

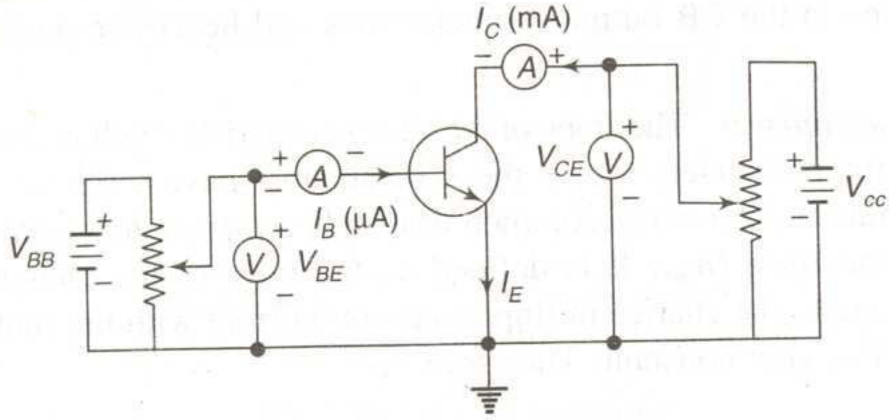


Fig. Circuit to determine CE Static characteristics.

Input Characteristics:

To determine the input characteristics, the collector to emitter voltage is kept constant at zero volts and base current is increased from zero in equal steps by increasing V_{BE} in the circuit. The value of V_{BE} is noted for each setting of I_B. This procedure is repeated for higher fixed values of V_{CE}, and the curves of I_B versus V_{BE} are drawn.

The input characteristics thus obtained are shown in figure below.

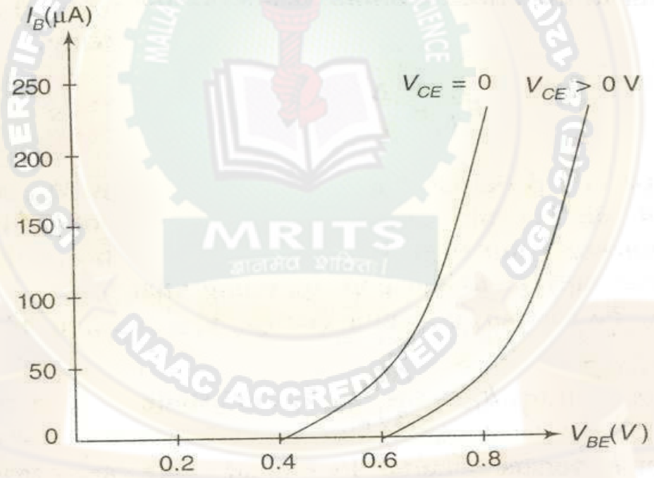


Fig. CE Input Characteristics.

When V_{CE}=0 , the emitter-base junction is forward biased and he junction behaves as a forward biased diode. When V_{CE} is increased, the width of the depletion region at the reverse biased collector-base junction will increase. Hence he effective width of the base will decrease. This effect causes a decrease in the base current I_B. Hence, to get the same value of I_B as that for V_{CE}=0, V_{BE} should be increased. Therefore, the curve shifts to the right as V_{CE} increases.

Output Characteristics:

To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting base-emitter voltage, V_{BE}. The magnitude of collector-emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting of V_{CE}. Now the curves of I_C versus V_{CE} are plotted for different constant values of I_B. The output characteristics thus obtained are shown in figure below.

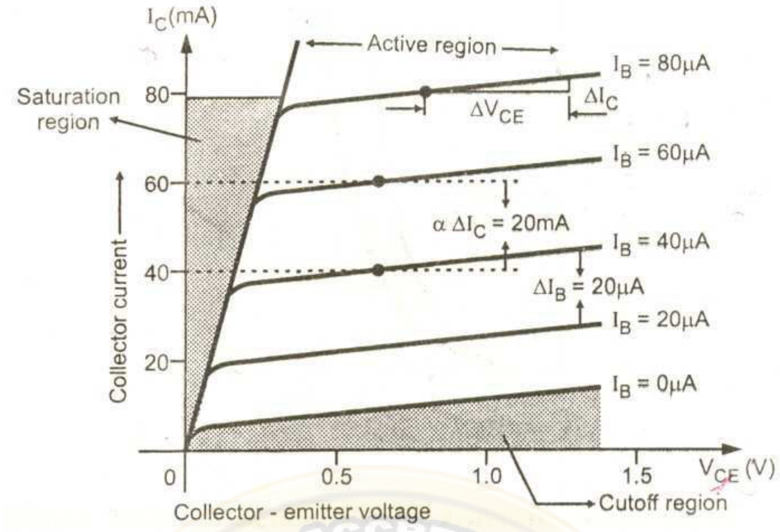


Fig. CE Output characteristics

The output characteristics of common emitter configuration consist of three regions: Active, Saturation and Cut-off regions.

Active Region: The region where the curves are approximately horizontal is the "Active" region of the CE configuration. In the active region, the collector junction is reverse biased. As V_{CE} is increased, reverse bias increase. This causes depletion region to spread more in base than in collector, reducing the changes of recombination in the base. This increase the value of α_{dc}. This Early effect causes collector current to rise more sharply with increasing V_{CE} in the active region of output characteristics of CE transistor.

Saturation Region: If V_{CE} is reduced to a small value such as 0.2V, then collector-base junction becomes forward biased, since the emitter-base junction is already forward biased by 0.7V. The input junction in CE configuration is base to emitter junction, which is always forward biased to operate transistor in active region. Thus input characteristics of CE configuration are similar to forward characteristics of p-n junction diode. When both the junctions are forwards biased, the transistor operates in the saturation region, which is indicated on the output characteristics. The saturation value of V_{CE}, designated $V_{CE(Sat)}$, usually ranges between 0.1V to 0.3V.

Cut-Off Region: When the input base current is made equal to zero, the collector current is the reverse leakage current I_{CEO}. Accordingly, in order to cut off the transistor, it is not enough to reduce I_B=0. Instead, it is necessary to reverse bias the emitter junction slightly. We shall define cut off as the condition where the collector current is equal to the reverse saturation current I_{CO} and the emitter current is zero.

Transistor Parameters:

The slope of the CE characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as Common emitter hybrid parameters (or) h-parameters.

i) Input Impedance (h_{ib}):

It is defined as the ratio of change in (input) base voltage to the change in (input) base current with the (output) collector voltage (V_{CE}), kept constant. Therefore,

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}$$, ΔV_{CE} constant

It is the slope of CB input characteristics I_B versus V_{BE}.

The typical value of h_{ie} ranges from 500Ω to 2000Ω.

ii) Output Admittance (h_{oe}):

It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage. With the (input) base current I_B kept constant. Therefore,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}$$, I_B constant

It is the slope of CE output characteristics I_C versus V_{CE}.

The typical value of this parameter is of the order of 0.1 to 10μmhos.

iii) Forward Current Gain (h_{fe}):

It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) base current keeping the (output) collector voltage V_{CE} constant. Hence,

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}$$, V_{CE} constant

It is the slope of I_C versus I_B curve.

Its typical value varies from 20 to 200.

iv) Reverse Voltage Gain (h_{re}):

It is defined as a ratio of the change in the (input) base voltage and the corresponding change in (output) collector voltage with constant (input) base current, I_B. Hence,

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}$$, I_E constant.

It is the slope of V_{BE} versus V_{CE} curve.

Its typical value is of the order of 10^{-5} to 10^{-4}.

Characteristics of common collector circuit:

The circuit diagram for determining the static characteristics of an N-P-N transistor in the common collector configuration is shown in fig. below.

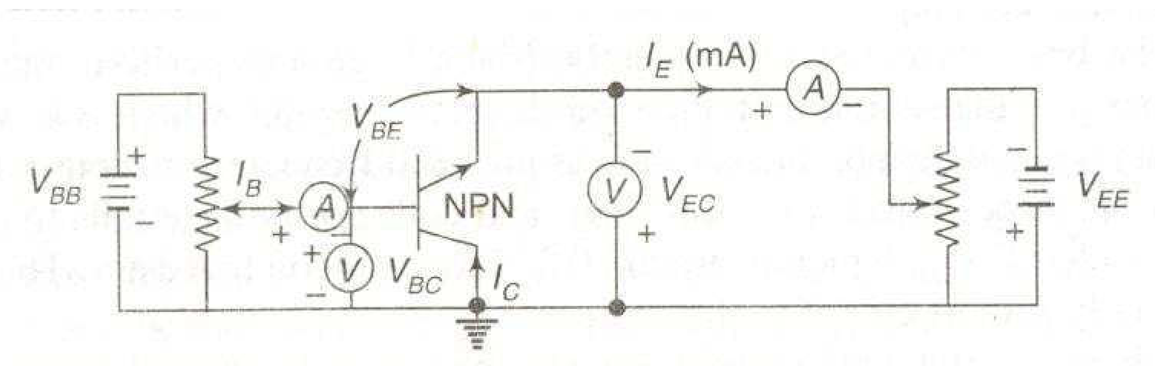


Fig. Circuit to determine CC static characteristics.

Input Characteristics:

To determine the input characteristic, V_{EC} is kept at a suitable fixed value. The base-collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC}. Plots of V_{BC} versus I_B for different values of V_{EC} shown in figure are the input characteristics.

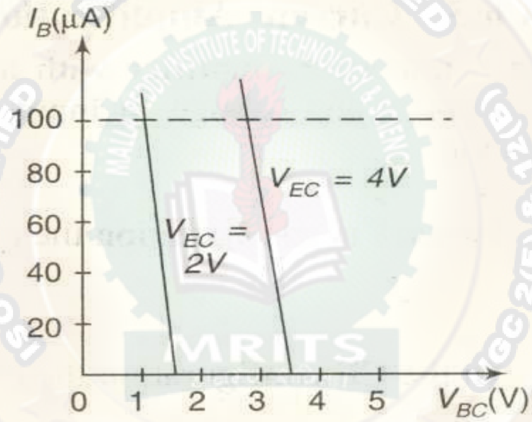


Fig. CC Input Characteristics.

Output Characteristics:

The output characteristics shown in figure below are the same as those of the common emitter configuration.

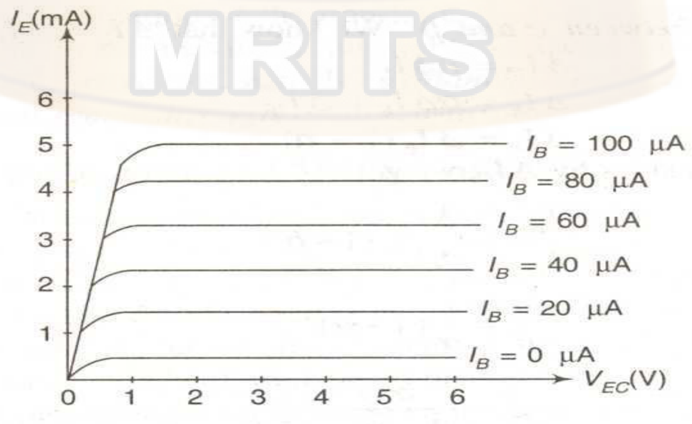


Fig. CC output characteristics.

Comparison:

Table: A comparison of CB, CE and CC configurations

Property	CB	CE	CC
Input Resistance	Low (About 100Ω)	Moderate (About 750Ω)	High (About 750kΩ)
Output Resistance	High (About 450kΩ)	Moderate (About 45kΩ)	Low (About 25Ω)
Current Gain	1	High	High
Voltage Gain	About 150	About 500	Less than 1
Phase Shift between input and output voltages	0^o (or) 360^o	180^o	0^o (or) 360^o
Applications	For high frequency circuits	For Audio frequency circuits	For impedance matching

Problem:

1 A Germanium transistor used in a complementary symmetry amplifier has I_{CBO}=10μA at 27°C and h_{fe}=50.

(a) find I_C when I_B=0.25mA and

(b) Assuming h_{fe} does not increase with temperature; find the value of new collector current, if the transistor's temperature rises to 50°C.

Solution:

Given data: I_{CBO} = 10μA and h_{fe} (=β) = 50

a) $I_C = \beta I_B + (1+\beta) I_{CBO}$

$= 50 \times (0.25 \times 10^{-3}) + (1+50) \times (10 \times 10^{-6})$A

=13.01mA

b) I'_{CBO} (β=50) $= I_{CBO} \times 2^{(T_2 - T_1)/10}$

$= 10 \text{ X } 2^{(50-27)/10}$

$= 10 \times 2^{2.3}$ μA

= 49.2μA

I_C at 50°C is

$I_C = \beta I_B + (1+\beta) I'_{CBO}$

$= 50 \times (0.25 \times 10^{-3}) + (1+50) \times (49.2 \times 10^{-6})$

=15.01 mA.

TRANSISTOR BIASING

Introduction:

The basic function transistor is to do amplification. The process of raising the strength of a weak signal without any change in its shape is known as faithful amplification.

For faithful amplification, the following three conditions must be satisfied:

i) The emitter-base junction should be forward biased,
ii) The collector-base junction should be reverse biased.
iii) Three should be proper zero signal collector current.

The proper flow of zero signal collector current (proper operating point of a transistor) and the maintenance of proper collector-emitter voltage during the passage of signal is known as 'transistor biasing'.

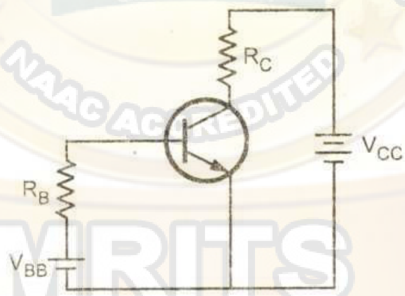
When a transistor is not properly biased, it work inefficiently and produces distortion in the output signal. Hence a transistor is to be biased correctly. A transistor is biased either with the help of battery (or) associating a circuit with the transistor. The latter method is generally employed. The circuit used with the transistor is known as biasing circuit.

In order to produce distortion-free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably chose. These voltages and resistances establish a set of d.c. voltage V_{CEQ} and current I_{CQ} to operate the transistor in the active region. These voltages and currents are called quiescent values which determine the operating point (or) Q-Point for the transistor.

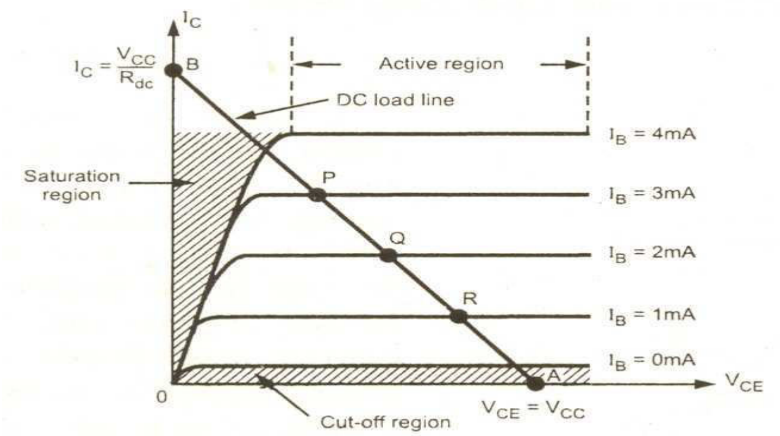
The process of giving proper supply voltages and resistances for obtaining the desired Q-Point is called biasing.

DC Load Line:

Consider common emitter configuration circuit shown in figure below:



In transistor circuit analysis generally it is required to determine the value of I_C for any desired value of V_{CE}. From the load line method, we can determine the value of I_C for any desired value of V_{CE}. The output characteristics of CE configuration is shown in figure below:



By applying KVL to the collector circuit

$$-V_C + I_C R_C + V_{CE} = 0$$

$$\Rightarrow V_{CC} = I_C R_C + V_{CE}$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

If the bias voltage V_{BB} is such that the transistor is not conducting then I_C=0 and V_{CE}= V_{CC}.

Therefore, when I_C=0, V_{CE}= V_{CC} this point is plotted on the output characteristics as point A.

If V_{CE}=0 then

$$0 = V_{CC} - I_C R_C$$

$$\Rightarrow I_C = \frac{V_{CC}}{R_C}$$

Therefore, V_{CE}=0, $I_C = \frac{V_{CC}}{R_C}$ this point is plotted on the output characteristics as point B. The line drawn through these points is straight line 'd.c load line'.

The d.c. load line is plot of I_C versus V_{CE} for a given value of R_C and a given level of V_{CC}. Hence from the load line we can determine the I_C for any desired value of V_{CE}.

Operating Point (or) Quiescent Point:

In designing a circuit, a point on the load line is selected as the dc bias point (or) quiescent point. The Q-Point specifies the collector current I_C and collector to emitter voltage V_{CE} that exists when no input signal is applied.

The dc bias point (or) quiescent point is the point on the load line which represents the current in a transistor and the voltage across it when no signal is applied. The zero signal values of I_C ad V_{CE} are known as the operating point.

Biasing:

The process of giving proper supply voltages and resistances for obtaining the desired Q-point is called 'biasing'.

How to choose the operating point on DC load line:

The transistor acts as an amplifier when it is operated in active region. After the d.c. conditions are established in the circuit, when an a.c. signal is applied to the input, the base current varies according to te amplitude of the signal and causes I_C to vary consequently producing an output voltage variation. This can be seen from output characterizes.

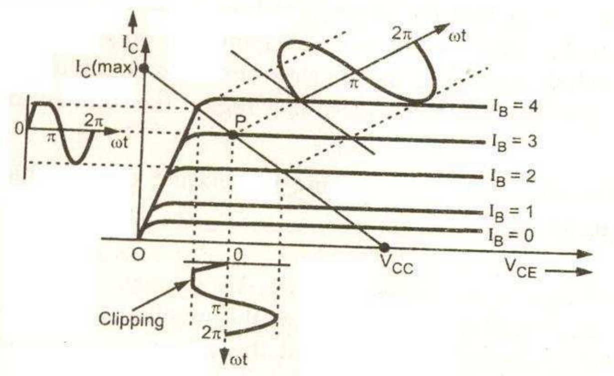


Fig. Operating point near saturation region gives clipping at the positive peak.

Consider point A which is very near to the saturation point, even though the base current is varying sinusoidally the output current and output voltage is seen to be clipped at the positive peaks. This results in distortion of the signal.

Consider point B which is very near to the cut-off region. The output signal is now clipped at the negative peak. Hence this two is not a suitable operating point.

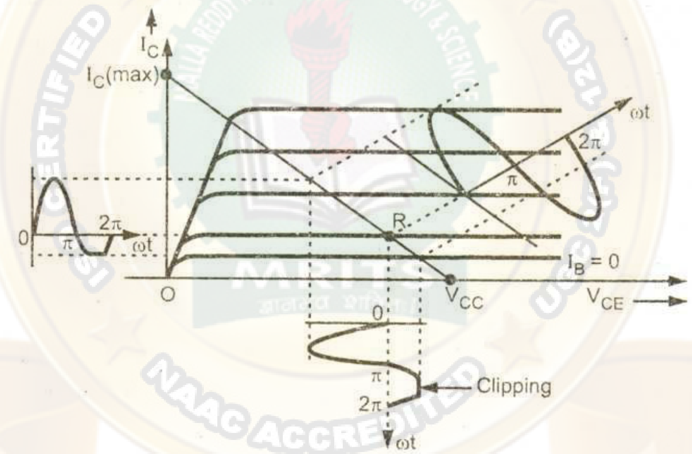


Fig. Operating point near cut-off region given clipping at the negative peak.

Consider point C which is the mid point of the DC load line then the output signal will not be distorted.

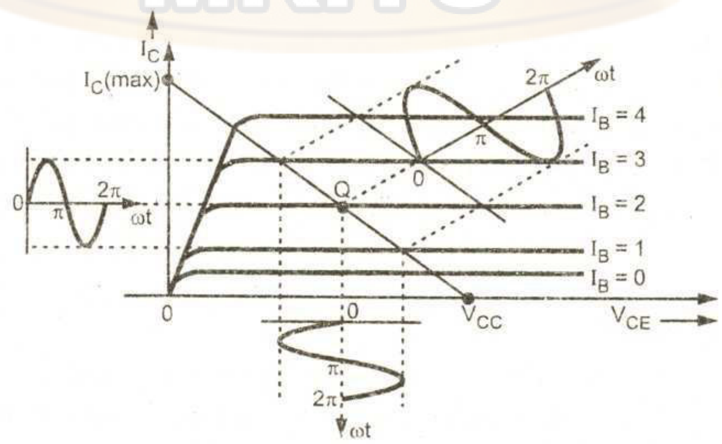


Fig. Operating point at the centre of active region is most suitable.

A good amplifier amplifies signals without introducing distortion. Thus always the operating point is chosen as the mid point of the DC load line.

Stabilization:

The maintenance of operating point stable is known as '*Stabilization'.*

There are two factors which are responsible for shifting the operating point. They are:

i) The transistor parameters are temperature dependent.
ii) When a transistor is replaced by another of same type, there is a wide spread in the values of transistor parameters.

So, stabilization of the operating point is necessary due to the following reasons:

i) Temperature dependence of I_C.

ii) Individual variations and

iii) Thermal runaway.

Temperature dependence of I_C:

The instability of I_C is principally caused by the following three sources:

i) The I_{CO} doubles for every 10°C rise in temperature.

ii) Increase of β with increase of temperature.

iii) The V_{BE} decreases about 2.5mV per °C increase in temperature.

Individual variations:

When a transistor is replaced by another transistor of the same type, the values of β and V_{BE} are not exactly the same. Hence the operating point is changed. So it is necessary to stabilize the operating point irrespective of individual variations in transistors parameters.

Thermal Runaway:

Depending upon the construction of a transistor, the collector junction can withstand maximum temperature. The range of temperature lies between 60°C to 100°C for 'Ge' transistor and 150°C to 225°C for 'Si' transistor. If the temperature increases beyond this range then the transistor burns out. The increase in the collector junction temperature is due to thermal runaway.

When a collector current flows in a transistor, it is heated i.e., its temperature increases. If no stabilization is done, the collector leakage current also increases. This further increases the transistor temperature. Consequently, there is a further increase in collector leakage current. The action becomes cumulative and the transistor may ultimately burn out. The self-destruction of an unstabilized transistor is known as thermal runaway.

The following two techniques are used for stabilization.

1) Stabilization techniques:

The technique consists in the use of a resistive biasing circuit which permits such a variation of base current I_B as to maintain I_C almost constant in spite of I_{CO}, β and V_{BE}.

2) Compensation techniques:

In this technique, temperature sensitive devices such as diodes, thermistors and sensistors etc., are used. Such devices produce compensating voltages and current in such a way that the operating points maintained stable.

Stability factors:

Since there are three variables which are temperature dependent, we can define three stability factors as below:

i) **<u>S:</u>** The stability factor 'S' is defined as the ration of change of collector current I_C with respect to the reverse saturation current I_{CO}, keeping β and V_{BE} constant i.e., $$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{\partial I_C}{\partial I_{CO}}\bigg|$$ V_{BE}, β constant

ii) <u>**S':**</u> The stability factor S' is defined as the rate of change of I_C with respect to V_{BE}, keeping I_{CO} and β constant i.e.,

$$S^{'} = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\partial I_C}{\partial V_{BE}}\bigg|$$ I_{CO}, β constant

iii) <u>**S'':**</u> The stability factor S'' is defined as the rate of change of I_C with respect to β, keeping I_{CO} and V_{BE} constant i.e.,

$$S^{'} = \frac{\partial I_C}{\partial \beta} \approx \frac{\partial I_C}{\partial \beta}\bigg|$$ I_{CO}, V_{BE} constant

Ideally, stability factor should be perfectly zero to keep operating point stable.

Practically, stability factor should have the value as minimum as possible.

Derivation of Stability Factor (S):

For a common emitter configuration collector current is given as,

$$I_C = \beta I_B + I_{CEO}$$
$$\Rightarrow I_C = \beta I_B + (1+\beta) I_{CO} \qquad \text{............. (1)}$$

Differentiating equation (1) w.r.t. I_C keeping β constant, we get

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta)\frac{\partial I_{CO}}{\partial I_C}$$

$$\Rightarrow 1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta)\frac{\partial I_{CO}}{\partial I_C}$$

$$\Rightarrow \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

$$\Rightarrow S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}} \qquad \text{........... (2)}$$

To obtain S' and S'':

In standard equation of I_C, replace I_B in terms of V_{BE} to get S'.
Differentiating equation of I_C w.r.t. β after replacing I_B in terms of V_{BE} to get S''.

Methods of Biasing:

Some of the methods used for providing bias for a transistor are as follows:

1) Fixed bias (or) base resistor method.
2) Collector to base bias (or) biasing with feedback resistor.
3) Voltage divider bias.

1). Fixed bias (or) base resistor method:

A CE amplifier used fixed bias circuit is shown in figure below:

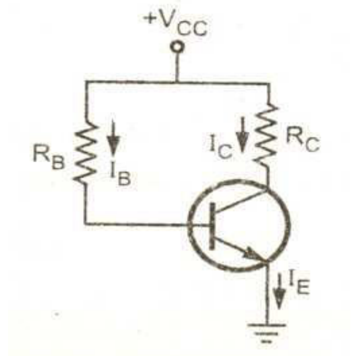


Fig. Fixed bias circuit.

In this method, a high resistance R_B is connected between positive terminal of supply V_{CC} and base of the transistor. Here the required zero signal base current flows through R_B and is provided by V_{CC}.

In figure, the base-emitter junction is forward biased because the base is positive w.r.t. emitter. By a proper selection of R_B, the required zero signal base current (and hence $I_C=\beta I_B$) can be made to flow.

Circuit Analysis:

Base Circuit:

Consider the base-emitter circuit loop of the above figure.

Writing KVL to the loop, we obtain

$$-V_{CC}+I_BR_B+V_{BE}=0$$

$$\Rightarrow V_{CC}=I_BR_B+V_{BE}$$

$$\Rightarrow I_B=\frac{V_{CC}-V_{BE}}{R_B}$$

But $I_C=\beta I_B+I_{CEO}$

As I_{CEO} is very small, $I_C\approx\beta I_B$

$$\therefore I_C=\beta\left(\frac{V_{CC}-V_{BE}}{R_B}\right)$$

$\Rightarrow$ β, V_{CC}, V_{BE} are constant for a transistor $\therefore$ I_C depends on R_B.

Choose suitable value of R_B to get constant I_C in active region.

$$\therefore R_B=\frac{(V_{CC}-V_{BE})\beta}{I_C} \quad \text{(or)} \quad R_B=\frac{\beta V_{CC}}{I_C} \qquad (\because V_{BE}<<V_{CC})$$

Collector Circuit:

Consider the collector-emitter circuit loop of the circuit.

Writing KVL to the collector circuit, we get

$$-V_{CC} + I_B R_B + V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

Stability factor S:

The stability factor S is given by, $S = \dfrac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_C}}$

We have $I_B = \dfrac{V_{CC} - V_{BE}}{R_B}$ = constant $\quad \therefore \dfrac{\partial I_B}{\partial I_C} = 0$

$$\therefore S = 1+\beta$$

If β=100 then S=101. This shows that I_C changes 101 times as much as any changes in I_{CO}. Thus I_C is dependent upon I_{CO} and temperature.

The value of S is high and has very poor stability.

Stability factor S':

We have $I_C = \beta I_B + (1+\beta) I_{CO}$

But $I_B = \dfrac{V_{CC} - V_{BE}}{R_B}$

$$\therefore I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right) + (1+\beta) I_{CO}$$

Differentiating the above equation w.r.t. I_C,

We get $1 = -\dfrac{\beta}{R_B}\dfrac{\partial V_{BE}}{\partial I_C}$

$$\Rightarrow S' = -\frac{\beta}{R_B}$$

Stability factor S'':

We have $I_C = \beta I_B + (1+\beta) I_{CO}$

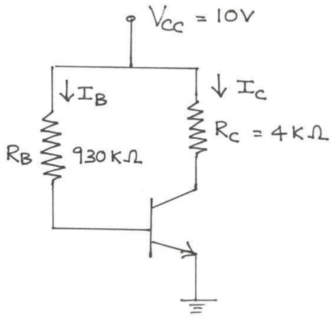
Differentiating the above equation w.r.t. β,

We get $\dfrac{\partial I_C}{\partial \beta} = I_B + I_{CO}$

$$\Rightarrow S'' = \frac{I_C}{\beta}$$ (∵ I_{CO} is very small & $I_B = \dfrac{I_C}{\beta}$)

Problem:

1) Figure below shows a silicon transistor with β=100 and biased by base resistor method. Determine the operating point.



Solution:

Given V_{CC}=10V, V_{BE}=0.7V (Silicon transistor), β=100, R_B=930kΩ.

Applying KVL to base-emitter loop, $V_{CC} - V_{BE} = I_B R_B \Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$$I_C = \beta I_B = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 100\left(\frac{10 - 0.7}{930 \times 10^3}\right) = 1mA$$

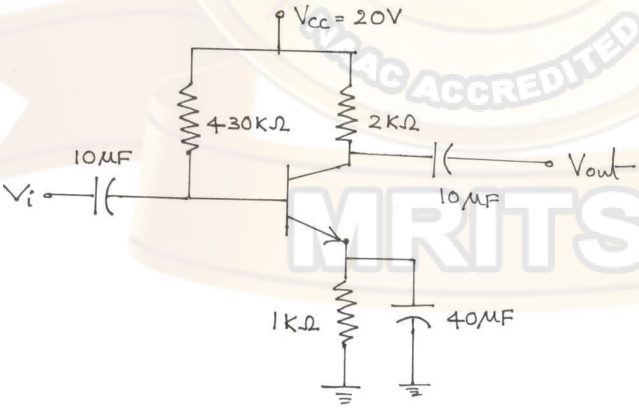
Applying KVL to collector-emitter loop,

$$V_{CC} - V_{CE} = I_C R_C \Rightarrow V_{CE} = V_{CC} - I_C R_C$$

$$\Rightarrow V_{CE} = 10 - \left(1 \times 10^{-3} \times 4 \times 10^3\right) = 6V$$

∴ Operating point is (6V, 1mA)

2. For the following circuit shown in figure below, find the operating point.



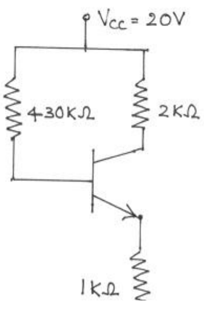
Solution:

DC equivalent of above circuit is shown below.

KVL to base-emitter loop is

$$-V_{CC} + I_B R_B + V_{BE} + \left(I_C + I_B\right) R_E = 0$$

$$I_B R_B + \beta I_B R_E + I_B R_B = V_{CC} - V_{BE}$$



$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$\therefore I_B = \frac{20 - 0.7}{(430 + 51) \times 10^3} = 40.1 \mu A$$

$$I_C = \beta I_B = 2.01 mA$$

KVL to collector-emitter loop is

$$-V_{CC} + I_C R_C + V_{CE} + I_C R_E = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$V_{CE} = 20 - 2.01 \times 10^{-3} (2+1) \times 10^3$ =20-6.03 = **13.97V**

∴ Operating point is **Q (13.97V, 2.01mA)**

Advantages of fixed bias circuit:

1. This is a simple circuit which uses very few components.
2. The operating point can be fixed anywhere in the active region of the characteristics by simply changing the values of R_B. Thus, it provides maximum flexibility in the design.

Disadvantages of fixed bias circuit:

1. With the rise in temperature the operating point if not stable.
2. When the transistor is replaced by another with different value of β, the operating point with shift i.e., the stabilization of operating point is very poor in fixed bias circuit.

Because of these disadvantages, fixed bias circuit required some modifications. In the modified circuit, R_B is connected between collector and base. Hence the circuit is called 'collector to base' bias circuit.

2). Collector to Base bias (or) Biasing with feedback resistor:

A CE amplifier using collector to base bias circuit is shown in the figure. In this method, the biasing resistor is connected between the collector and the base of the transistor.

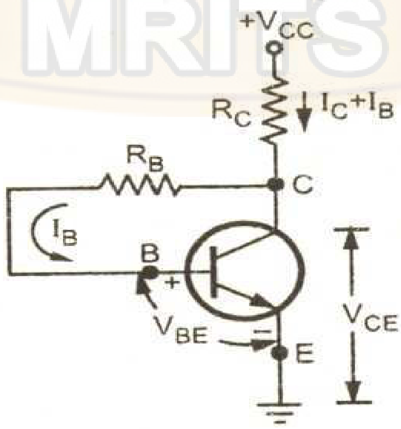


Fig. Collector–to–Base bias circuit.

Circuit Analysis:

Base Circuit:

Consider the base-emitter circuit, applying the KVL to the circuit we get,

$$V_{CC} - \left(I_B + I_C\right)R_C - I_B R_B - V_{BE} = 0$$

$$\Rightarrow V_{CC} = I_B\left(R_C + R_B\right) + I_C R_C + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \qquad \text{................ (1)}$$

But $I_C = \beta I_B$

$$\therefore I_C = \frac{\beta\left(V_{CC} - I_C R_C - V_{BE}\right)}{R_C + R_B} \qquad \text{................ (2)}$$

Collector circuit:

Consider the collector-emitter circuit, applying the KVL to the circuit we get

$$-V_{CC} + \left(I_B + I_C\right)R_C + V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - \left(I_C + I_B\right)R_C \qquad \text{............... (3)}$$

Stability factor S:

The stability factor S is given by,

$$S = \frac{1+\beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

We have $I_B = \dfrac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$ = constant

Differentiating the above equation w.r.t. I_C we get

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_C + R_B}$$

$$\therefore S = \frac{1+\beta}{1 + \beta \frac{R_C}{R_C + R_B}} \qquad \text{................. (4)}$$

The stability factor S is smaller than the value obtained by fixed bias circuit. Also 'S' can be made smaller by making R_B small (or) R_C large.

Stability factor S':

We have $I_C = \dfrac{\beta\left(V_{CC} - V_{BE} - I_C R_C\right)}{R_C + R_B}$

Differentiating the above equation w.r.t. I_C,

We get $$1 = -\frac{\beta}{R_B + R_C}\frac{\partial V_{BE}}{\partial I_C} - \beta\frac{R_C}{R_B + R_C}$$

$$1 + \beta\frac{R_C}{R_B + R_C} = -\frac{\beta}{R_B + R_C}\frac{\partial V_{BE}}{\partial I_C}$$

$$\frac{R_C + R_B + \beta R_C}{R_C + R_B} = -\frac{\beta}{R_C + R_B}\frac{\partial V_{BE}}{\partial I_C}$$

$$\Rightarrow S' = -\frac{\beta}{R_B + (1+\beta)R_C} \quad \text{......................... (5)}$$

Stability factor S'':

We have $I_C = \dfrac{\beta\left(V_{CC} - V_{BE} - I_C R_C\right)}{R_C + R_B}$

Differentiating the above equation w.r.t. β,

We get $$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC} - V_{BE}}{R_C + R_B} - \frac{R_C}{R_C + R_B}\left[I_C + \beta\frac{\partial I_C}{\partial \beta}\right]$$

$$\Rightarrow \frac{\partial I_C}{\partial \beta}\left[1 + \beta\frac{R_C}{R_C + R_B}\right] = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B}$$

$$\Rightarrow \frac{\partial I_C}{\partial \beta}\left[R_B (1+\beta) R_C\right] = V_{CC} - V_{BE} - I_C R_C$$

$$\Rightarrow S'' = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + (1+\beta)R_C}$$

$$\Rightarrow S'' = \frac{I_C\left(R_C + R_B\right)}{R_B + (1+\beta)R_C} \quad \text{.................. (6)}$$

Problems:

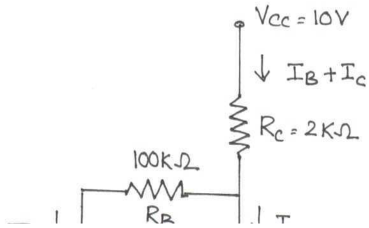
3. An N-P-N transistor with β=50 is used in a CE circuit with V_{CC}=10V, R_C=2kΩ. The bias is obtained by connecting a 100kΩ resistance from collector to base. Assume V_{BE}=0.7V. Find

i) the quiescent point and

ii) Stability factor 'S'

Solution:

i) Applying KVL to the base circuit,



$$V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE}$$
$$\Rightarrow V_{CC} = I_B(R_C + R_B) + I_C R_C + V_{BE}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \quad \therefore I_C = \frac{\beta(V_{CC} - V_{BE} - I_C R_C)}{R_C + R_B}$$

$$\therefore I_C = \frac{50(10 - 0.7 - 2\times10^{-3} I_C)}{102\times10^3} \qquad \Rightarrow I_C = 2.3mA$$

Applying KVL to the collector circuit,

$$V_{CC} = (I_B + I_C)R_C + V_{CE} \qquad \therefore V_{CE} = V_{CC} - (I_B + I_C)R_C$$
$$= 10 - (46\times10^{-6} + 2.3\times10^{-3})\times2\times10^3$$

$\Rightarrow V_{CE} = 5.308V$ $\therefore$ The quiescent point is **(5.308V, 2.3mA)**

ii) Stability factor, S:

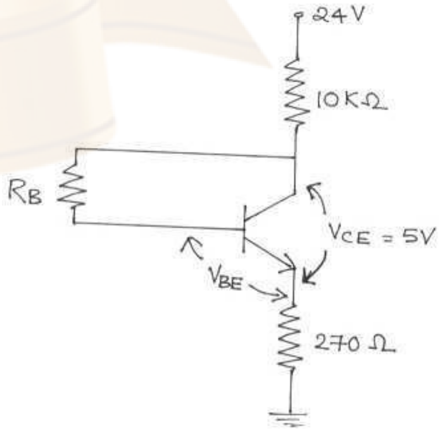
$$S = \frac{1+\beta}{1+\beta\dfrac{R_C}{R_C+R_B}}$$

$$\Rightarrow S = \frac{51}{1+50\left(\dfrac{20\times10^3}{102\times10^3}\right)} = 25.75$$

4. A transistor with β=45 is used with collector to base resistor R_B biasing with quiescent value of 5V for V_{CE}. If V_{CC}=24V, R_C=10kΩ, R_E=270Ω, find the value of R_B.

Solution:

Applying KVL to collector and emitter loop, we have



$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$
$$\Rightarrow V_{CC} - V_{CE} = I_C R_C + (I_C + I_B)R_E$$
$$\Rightarrow V_{CC} - V_{CE} = [\beta R_C + (1+\beta)R_E] I_B$$
$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{\beta R_C + (1+\beta)R_E} = \frac{24-5}{45\times10 + 50\times0.27}$$

=0.041 mA

Further, $V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$

$$\Rightarrow V_{CC} - V_{BE} = R_C \beta I_B + I_B R_B + (1+\beta)R_E I_B$$

$$\Rightarrow 24 - 0.7 = I_B[45\times10 + R_B + 50\times0.27] \qquad \Rightarrow 23.3 = 0.041[450 + R_B + 12.42]$$

$$\therefore R_B = 105.87 K\Omega$$

3). Voltage Divider Bias (Or) Self-Bias (Or) Emitter Bias:

The voltage divider bias circuit is shown in figure.

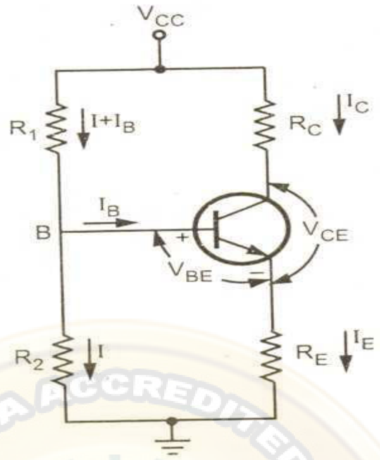


Fig. Voltage divider bias circuit.

In this method, the biasing is provided by three resistors R_1, R_2 and R_E. The resistors R_1 and R_2 acts as a potential divider giving a fixed voltage to the base.

If collector current increases due to change in temperature (or) change in β, the emitter current I_E also increases and the voltage drop across R_E increases, reducing the voltage difference between base and emitter (V_{BE}).

Due to reduction in V_{BE}, base current I_B and hence collector current I_C is also reduces. Therefore, we can say that negative feedback exists in the emitter bias circuit. This reduction in collector current I_C components for the original change in I_C.

Circuit Analysis:

Let current flows through R_1. As the base current I_B is very small, the current flowing through R_2 can also be taken as I.

The calculation of collector current I_C is as follows:

The current 'I' flowing through R_1 (or) R_2 is given by $I = \frac{V_{CC}}{R_1 + R_2}$ .... (1)

The voltage V_2 developed across R_2 is given by, $V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$ .... (2)

Base Circuit:

Applying KVL to the base circuit, we have

$$V_2 = V_{BE} + V_E = V_{BE} + I_E R_E \qquad \Rightarrow V_2 = V_{BE} + I_C R_E \qquad (\because I_E \approx I_C)$$

$$\therefore I_C = \frac{V_2 - V_{BE}}{R_E} \quad \text{................ (3)}$$

Hence I_C is almost independent of transistor parameters and hence good stabilization is ensured.

Collector Circuit:

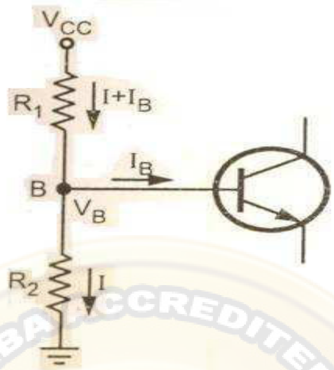
Applying KVL to the collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \qquad \Rightarrow V_{CC} = I_C R_C + V_{CE} + I_C R_E \qquad \left(\because I_E \approx I_C\right)$$

$$\Rightarrow V_{CE} = V_{CC} - I_C\left(R_C + R_E\right) \qquad \text{.................. (4)}$$

Circuit analysis using Thevenin's Theorem:

The Thevenin equivalent circuit of voltage-divider bias is as shown below:



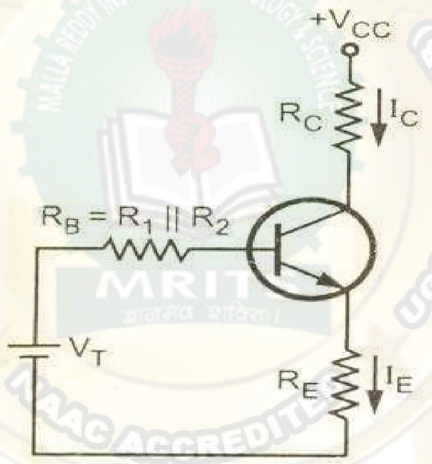


Fig. Simplified equivalent circuit.

From above figure we have,

$$V_2 = V_{Th} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} \qquad \text{.................... (5)}$$

$$R_{Th} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} \qquad \text{.................... (6)}$$

Applying KVL to the base-emitter circuit, we have

$$V_{Th} = I_B R_{Th} + V_{BE} + \left(I_B + I_C\right) R_E \qquad \text{................... (7)}$$

Applying KVL to the collector-emitter circuit, we have

$$V_{CE} = V_{CC} - I_C\left(R_C + R_E\right) \quad \left(\because I_C >> I_B\right)$$

………………... (8)

From equation (8), we have

$$\therefore I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

Substituting this value of I_C in equation (7), we have

$$V_{Th} = I_B R_{Th} + V_{BE} + R_E \left[I_B + \frac{V_{CC} - V_{CE}}{R_C + R_E} \right]$$

(or) $$V_{Th} = I_B R_{Th} + V_{BE} + R_E I_B + \frac{R_E V_{CC}}{R_C + R_E} - \frac{R_E V_{CE}}{R_C + R_E}$$

From equation (9) we can calculate the value of collector voltage V_{CE} for each value of I_B.

Stability factor (S):

For determining stability factor 'S' for voltage divider bias, consider the Thevenin's equivalent circuit.

Hence, Thevenin's equivalent voltage V_{Th} is given by

$$V_{Th} = \frac{R_2}{R_1 + R_2} V_{CC}$$

and the R_1 and R_2 are replaced by R_B which is the parallel combination of R_1 and R_2.

$$\therefore R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Applying KVL to the base circuit, we get $$V_{Th} = I_B R_B + V_{BE} + \left(I_B + I_C\right) R_E$$

Differentiating w.r.t. I_C and considering V_{BE} to be independent of I_C we get,

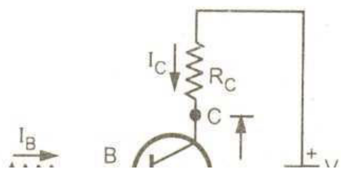
$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C}\left(R_E\right) + R_E$$

$$\therefore \frac{\partial I_B}{\partial I_C}\left(R_E + R_B\right) = -R_E \qquad \therefore \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B}$$

We have already seen the generalized expression for stability factor 'S' given by

$$S = \frac{1+\beta}{1-\beta \dfrac{\partial I_B}{\partial I_C}}$$

Substituting value of $\frac{\partial I_B}{\partial I_C}$ in the above equation, we get



$$\therefore S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}$$

$$\Rightarrow S = \frac{(1+\beta)(R_E+R_B)}{R_B+R_E+\beta R_E} = \frac{(1+\beta)(R_E+R_B)}{R_B+(1+\beta)R_E}$$

$$S = (1+\beta)\left(\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}}\right)$$

The ratio $\frac{R_B}{R_E}$ controls value of stability factor 'S'.

If $\frac{R_B}{R_E} << 1$ then above equation reduces to $S = (1+\beta)\left(\frac{1}{1+\beta}\right) = 1$

Practically $\frac{R_B}{R_E} \neq 0$ But to have better stability factor 'S', we have to keep ration $\frac{R_B}{R_E}$ as small as possible.

Stability factor 'S' for voltage divider bias (or) self bias is less as compared to other biasing circuits studied. So, this circuit is most commonly used.

Stability factor (S'):

Stability factor S' is given by $S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|$ I_{CO}, β constant

It is the variation of I_C with V_{BE} when I_{CO} and β are considered constant.

We know that, $I_C = \beta I_B + (1+\beta) I_{CO}$

$$I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta}$$

and $V_{Th} = I_B R_B + V_{BE} + (I_B + I_C) R_E$

$$V_{BE} = V_{Th} - (R_E + R_B) I_B - R_E I_C$$

By substituting I_B in the above equation, we get

$$V_{BE} = V_{Th} - (R_E+R_B)\left(\frac{I_C - (1+\beta) I_{CO}}{\beta}\right) - R_E I_C$$

$$= V_{Th} - \frac{(R_E+R_B) I_C}{\beta} + \frac{(R_E+R_B)(1+\beta) I_{CO}}{\beta} - R_E I_C$$

$$\Rightarrow V_{BE} = V_{Th} - \frac{\left[(1+\beta)R_E + R_B\right]I_C}{\beta} + \frac{\left(R_E + R_B\right)(1+\beta)I_{CO}}{\beta}$$

Differentiating the above equation w.r.t V_{BE} with I_{CO} and β constant, we get

$$1 = 0 - \left[\frac{R_B + (1+\beta)R_E}{\beta}\right]\frac{\partial I_C}{\partial V_{BE}} + 0$$

$$\Rightarrow \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (1+\beta)R_E}$$

$$\therefore S' = \frac{-\beta}{R_B + (1+\beta)R_E}$$

Stability Factor S'':

Stability factor S'' is given by $S'' = \left.\frac{\partial I_C}{\partial \beta}\right|$ I_{CO}, V_{BE} constant

We have, $$V_{BE} = V_{Th} - \frac{\left[R_B + (1+\beta)R_E\right]I_C}{\beta} + \left[\frac{\left(R_E + R_B\right)(1+\beta)}{\beta}\right]I_{CO}$$

$$= V_{Th} - \frac{\left[R_B + (1+\beta)R_E\right]I_C}{\beta} + V'$$

Where $V' = \left[\frac{\left(R_E + R_B\right)(1+\beta)}{\beta}\right]I_{CO} = \left(R_E + R_B\right)I_{CO}$ $(\because \beta >> 1)$

Therefore, we write the above equation in terms of I_C, we get

$$I_C = \frac{\beta\left[V_{Th} + V' - V_{BE}\right]}{R_B + R_E(1+\beta)}$$

Differentiating above equation w.r.t. taking V' independent of β, we get,

$$\frac{\partial I_C}{\partial \beta} = \frac{R_B + R_E(1+\beta)\left(V_{Th} + V' - V_{BE}\right) - \beta\left[V_{Th} + V' - V_{BE}\right]R_E}{\left[R_B + R_E(1+\beta)\right]^2}$$

Multiplying numerator and denominator by (1+β) we get,

$$\frac{\partial I_C}{\partial \beta} = \frac{(1+\beta)\left(R_B + R_E\right)\left(V_{Th} + V' - V_{BE}\right)}{(1+\beta)\left[R_B + R_E(1+\beta)\right]\left[R_B + R_E(1+\beta)\right]}$$

$$= \frac{S\left(V_{Th} + V' - V_{BE}\right)}{(1+\beta)\left[R_B + R_E(1+\beta)\right]} \qquad \left\{\because S = \frac{(1+\beta)\left(R_B + R_E\right)}{\left[R_B + R_E(1+\beta)\right]}\right\}$$

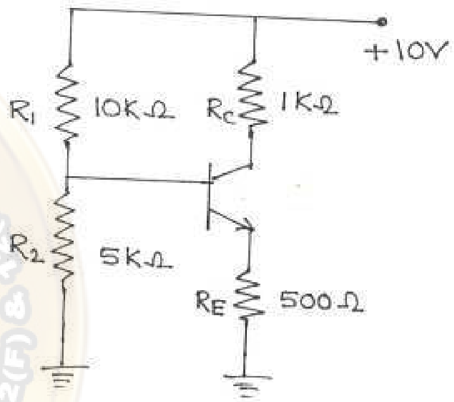
Multiplying numerator and denominator by β, we get

$$\frac{\partial I_C}{\partial \beta} = \frac{\beta\left(V_{Th} + V' - V_{BE}\right)S}{\beta(1+\beta)\left[R_B + R_E(1+\beta)\right]} = \frac{I_C S}{\beta(1+\beta)}$$

$$\left(\because I_C = \frac{\beta\left(V_{Th} + V' - V_{BE}\right)}{\left[R_B + R_E(1+\beta)\right]}\right) \qquad \therefore S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C S}{\beta(1+\beta)} \text{ where } S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}.$$

Problems:

5. For the circuit shown in figure, determine the value of I_C and V_{CE}. Assume V_{BE}=0.7V and β=100



Solution: $$V_B = \frac{R_1}{R_1+R_2}V_{CC} = \frac{5\times10^3}{10\times10^3+5\times10^3}\times10 = 3.33V$$

We know that $V_E = V_B - V_{BE} = 3.33 - 0.7 = 2.63V$

and $I_E = \frac{V_E}{R_E} = \frac{2.63V}{500} = 5.26mA$

We know that $I_B = \frac{I_E}{1+\beta} = \frac{2.63\times10^{-3}}{101} = 52.08\mu A$

and $I_C=\beta I_B=100\times52.08\times10^{-6}$ = **5.208mA**

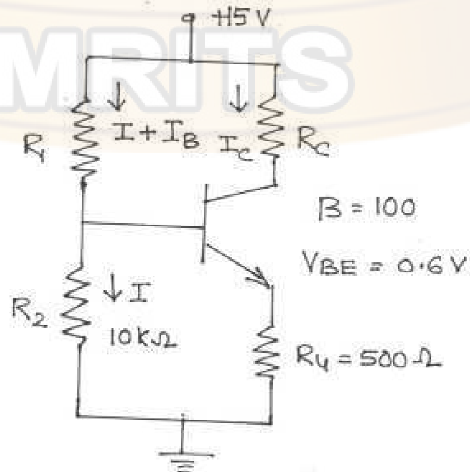
Applying KVL to the collector circuit we get

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C - I_E R_E \quad =10-5.208\times10^{-3}\times1\times10^{3}- 5.26\times10^{-3}\times500$$

$$\Rightarrow V_{CE} = 2.162V$$

6. In the circuit shown, if I_C=2mA and V_{CE}=3V, Calculate R_1 and R_3.



Solution:

From collector circuit,

$15 = I_C R_3 + V_{CE} + I_E R_4$

$= 2\times10^{-3}\times R_3 + 3 + (1+\beta) I_B \times 500$

$$\Rightarrow 12 = 2\times10^{-3}\times R_3 + 101\times\frac{2\times10^{-3}}{100}\times500$$

$$\Rightarrow R_3 = 5.495k\Omega$$

From Base circuit, $V_2 = \frac{R_2}{R_1+R_2}V_{CC}$

$$\Rightarrow V_2 = \frac{10\times10^{-3}}{R_1+10\times10^{-3}}\times15$$

But, $V_2 = V_{BE}+V_E = 0.6 + I_E R_4 = 0.6 + (1+\beta) I_B R_4$

$$\Rightarrow V_2 = 0.6 + 101\times\frac{2\times10^{-3}}{100}\times500 = 1.61V$$

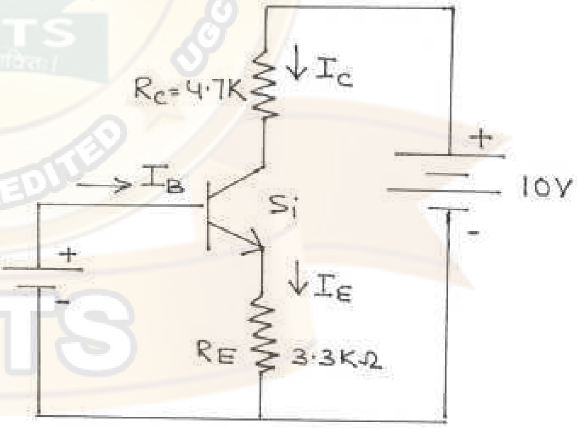
$$\therefore 1.61 = \frac{1\times10^{-3}}{R_1+10\times10^{-3}}\times15$$

$$\Rightarrow R_1 + 10\times10^{-3} = 93.17\times10^3$$

$$\Rightarrow R_1 = 83.17k\Omega$$

7. For the circuit shown below, calculate V_E, I_E, I_C and V_C. Assume V_{BE}=0.7V.

Solution:



From Base circuit,

$$4 = V_{BE} + V_E = 0.7 + V_E$$

$$\Rightarrow V_E = 3.3V$$

$$I_E R_E = 3.3$$

$$\Rightarrow I_E = \frac{3.3}{3.3\times10^3} = 1mA$$

But $I_E=I_B+I_C = (1+\beta)I_B$

Assume β=100,

$$\Rightarrow I_B = \frac{1mA}{101} = 0.0099mA$$

$I_C=\beta I_B$ = 100x0.0099mA = **0.99mA**

From Collector circuit,

$$V_C = 10 - I_C R_C = 100 - 0.99mA\times4.7K\Omega = 5.347V$$

Bias Compensation Techniques:

The biasing circuits provide stability of operating point in case variations in the transistor parameters such as I_{CO}, V_{BE} and β.

The stabilization techniques refer to the use of resistive biasing circuits which permit I_B to vary so as to keep I_C relatively constant.

On the other hand, compensation techniques refer to the use of temperature sensitive devices such as diodes, transistors, thermistors, sensistors etc., to compensate for the variation in currents. Sometimes for excellent bias and thermal stabilization, both stabilization as well as compensation techniques are used.

The following are some compensation techniques:

1) Diode compensation for instability due to V_{BE} variation.
2) Diode compensation for instability due to I_{CO} variation.
3) Thermistor compensation.
4) Sensistor compensation.

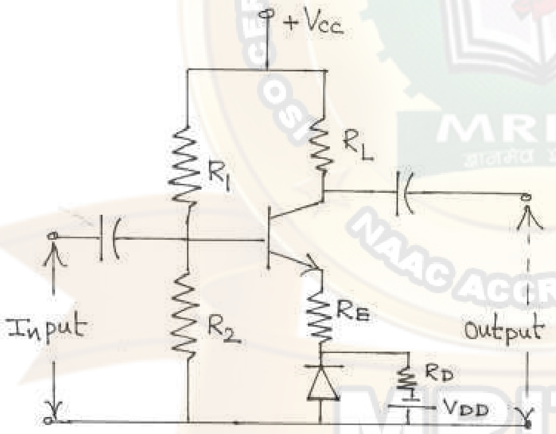
1) Diode compensation for instability due to V_{BE} variation:

For germanium transistor, changes in I_{CO} with temperature contribute more serious problem than for silicon transistor.

On the other hand, in a silicon transistor, the changes of V_{BE} with temperature possesses significantly to the changes in I_C.

A diode may be used as compensation element for variation in V_{BE} (or) I_{CO}.

The figure below shows the circuit of self bias stabilization technique with a diode compensation for V_{BE}. The Thevenin's equivalent circuit is shown in figure.



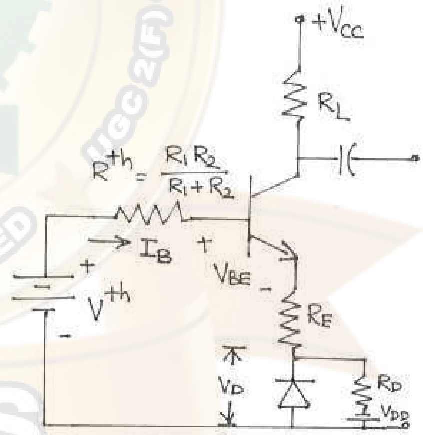


Fig. Self bias with stabilization and compensation Fig. Thevenin's equivalent circuit

The diode D used here is of the same material and type as the transistor. Hence the voltage V_D across the diode has same temperature coefficient (-2.5mV/°C) as V_{BE} of the transistor. The diode D is forward biased by the source V_{DD} and resistor R_D.

Applying KVL to the base circuit, we get

$$-V_{Th} + I_B R_{Th} + V_{BE} + I_E R_E - V_D = 0$$

$$\Rightarrow V_{Th} - V_{BE} + V_D = I_B R_{Th} + R_E\left(I_E + I_C\right) \quad \text{.................... (1)}$$

But $$I_C = \beta I_B + \left(1+\beta\right) I_{CO} \quad \text{.................. (2)}$$

From equation (1), we get

$$V_{Th} - V_{BE} + V_D = R_E I_C + \left(R_{Th} + R_E\right) I_B$$

Substituting the value of I_B from equation (2), we get

$$V_{Th} - V_{BE} + V_D = R_E I_C + \left(R_{Th} + R_E\right)\left(\frac{I_C - (1+\beta) I_{CO}}{\beta}\right)$$

$$\Rightarrow \beta\left(V_{Th} - V_{BE} + V_D\right) = \beta R_E I_C + \left(R_{Th} + R_E\right) I_C - (1+\beta) I_{CO}\left(R_{Th} + R_E\right)$$

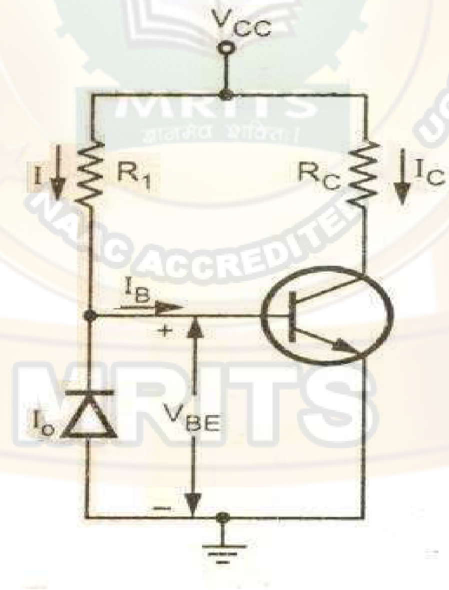
$$\Rightarrow \beta\left(V_{Th} - V_{BE} + V_D\right) = (1+\beta) I_{CO}\left(R_{Th} + R_E\right) = I_C\left(R_{Th} + (1+\beta) R_E\right)$$

$$\Rightarrow I_C = \frac{\beta\left(V_{Th} - V_{BE} + V_D\right) = (1+\beta) I_{CO}\left(R_{Th} + R_E\right)}{R_{Th} + (1+\beta) R_E} \qquad \text{.............. (3)}$$

Since variation in V_{BE} with temperature is the same as the variation in V_D with temperature, hence the quantity (V_{BE}-V_D) remains constant in equation (3). So the current I_C remains constant in spite of the variation in V_{BE}.

2) Diode compensation for instability due to I_{CO} variation:

Consider the transistor amplifier circuit with diode D used for compensation of variation in I_{CO}. The diode D and the transistor are of the same type and same material.



In this circuit diode is kept in reverse biased condition.

The reverse saturation current I_O of the diode will increase with temperature at the same as the transistor collector saturation current I_{CO}.

From figure $I = \frac{V_{CC} - V_{BE}}{R} \approx \frac{V_{CC}}{R}$ = constant.

The diode D is reverse biased by V_{BE}. So the current through D is the reverse saturation current I_O. Now base current I_B=I-I_O

But $I_C = \beta I_B + (1+\beta) I_{CO}$

$$\Rightarrow I_C = \beta\left(I - I_O\right) + \left(1+\beta\right) I_{CO}$$

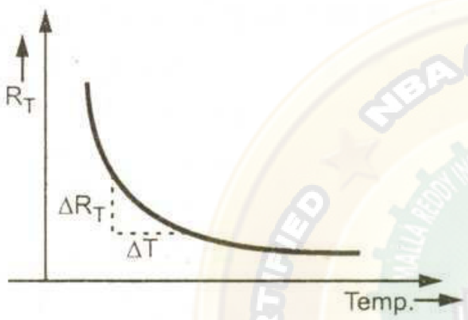
If β>>1, $I_C \approx \beta I - \beta I_O + \beta I_{CO}$

In the above expression, I is almost constant and if I_O of diode D and I_{CO} of transistor track each other over the operating temperature range, then I_C remains constant.

3) Thermistor Compensation:

This method of transistor compensation uses temperature sensitive resistive elements, thermistor rather than diodes (or) transistors:

It has a negative temperature coefficient, its resistance decreases exponentially with increasing temperature as shown in the figure.



Slope of this curve $= \frac{\partial R_T}{\partial T}$

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor, and the slope is negative. So we can say that thermistor has negative temperature coefficient of resistance.

Figure below shows thermistor compensation technique.

As shown in figure, R_2 is replaced by thermistor R_T in self bias circuit.

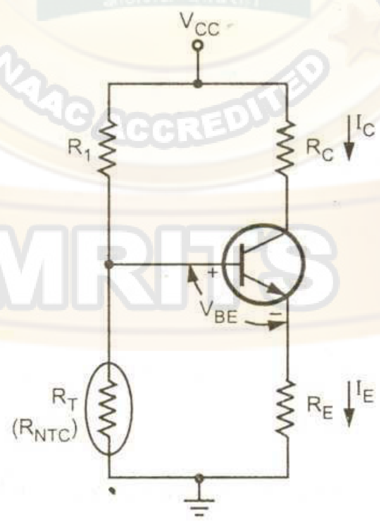


Fig. Thermistor compensation technique.

With increase in temperature, R_T decreases. Hence voltage drop across it also decreases. This voltage drop is nothing but the voltage at the base with respect to ground. Hence, V_{BE} decreases which reduces I_B. This behavior will tend to offset the increase in collector current with temperature.

We know, $I_C = \beta I_B + \left(1+\beta\right) I_{CO}$

In this equation, there is increase in I_{CBO} and decreases in I_B which keeps I_C almost constant.

Consider another thermistor compensation technique shown in figure. Here, thermistor is connected between emitter and V_{CC} to minimize the increase in collector current due to change in I_{CO}, V_{BE} (or) β with temperature.

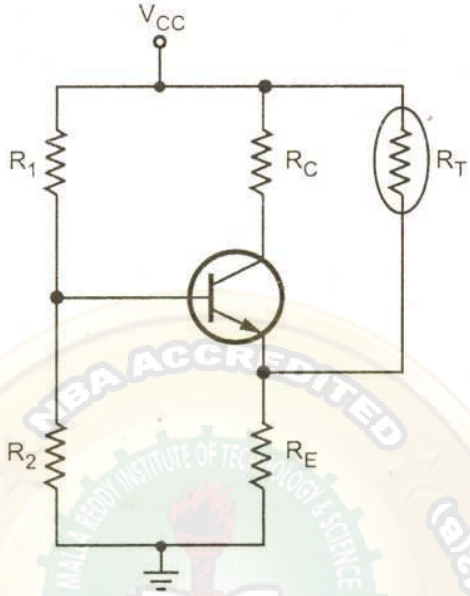


Fig. Thermistor compensation technique.

I_C increase with temperature and R_T decreases with increase in temperature. Therefore, current flowing through R_E increases, which increases the voltage drop across it. Emitter to Base junction is forward biased. But due to increase in voltage drop across R_E, emitter is made more positive, which reduces the forward bias voltage V_{BE}. Hence, base current reduces.

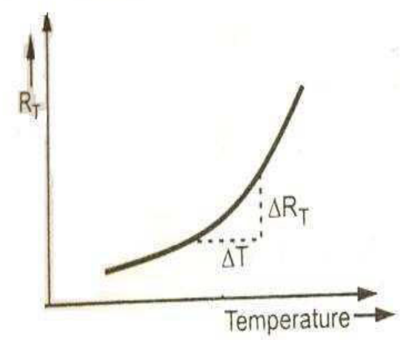
I_C is given by, $I_C = \beta I_B + (1+\beta) I_{CO}$

As I_{CBO} increases with temperature, I_B decreases and hence I_C remain fairly constant.

4) Sensistor Compensation:

This method of transistor compensation uses sensistor, which is temperature sensitive resistive element.

Sensistor has a positive temperature coefficient, i.e., its resistance increases exponentially with increasing temperature.



Slope of this curve $= \frac{\partial R_T}{\partial T}$

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for sensistor, and the slope is positive.

So we can say that sensistor has positive temperature coefficient of resistance.

As shown in figure R_1 is replaced by sensistor R_T in self bias circuit.

As temperature increases, R_T increases which decreases the current flowing through it. Hence current through R_2 decreases which reduces the voltage drop across it.

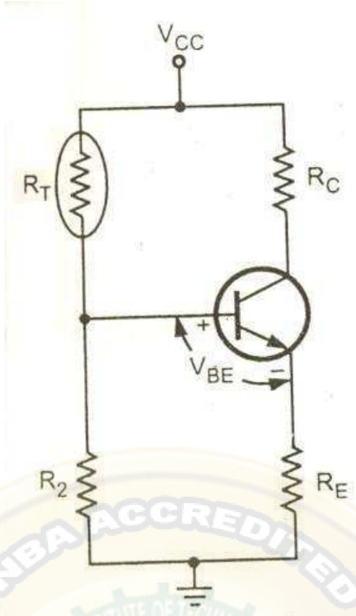


Fig. Sensistor compensation technique.

As voltage drop across R_2 decreases, I_B decreases. It means, when I_{CBO} increases with increase in temperature, I_B reduces due to variation in V_{BE}, maintaining I_C fairly constant.

Thermal Runaway:

The collector current for the CE circuit is given by

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

The three variables in the equation, β, I_B and I_{CO} increase with rise in temperature. In particular, the reverse saturation current (or) leakage current I_{CO} changes greatly with temperature. Specifically, it doubles for every 10°C rise in temperature.

The collector current I_C causes the collector-base junction temperature to rise which, in turn, increase I_{CO}, as a result I_C increase still further, which will further rise the temperature at the collector-base junction. This process is cumulative and it is referred to as self heating.

The excess heat produced at the collector-base junction may even burn and destroy the transistor. This situation is called "Thermal Runaway" of the transistor.

Thermal Resistance:

Transistor is a temperature dependent device.

In order to keep the temperature within the limits, the heat generated must be dissipated to the surroundings.

Most of the heat within the transistor is produced at the collector junction.

If the temperature exceeds the permissible limit, the junction is destroyed.

For Silicon transistor, the temperature is in the range 150°C to 225°C.

For Germanium, it is between 60°C to 100°C.

Let T_A°C be the ambient temperature i.e., the temperature of surroundings air around transistor and T_j°C, the temperature of collector-base junction of the transistor.

Let P_D be the power in watt dissipated at the collector junction.

The steady state temperature rise at the collector junction is proportional to the power dissipated at the junction. It is given by

$$\partial T = T_j - T_A = \theta P_D$$ Where θ = constant of proportionality

The θ, which is constant of proportionality, is referred to as thermal resistance.

$$\theta = \frac{T_j - T_A}{P_D}$$

The unit of θ, the thermal resistance, is ^oC/watt.

The typical values of θ for various transistors vary from 0.2^oC/watt for a high power transistor to 1000 ^oC/watt for a low power transistor.

Heat Sink:

As power transistors handle large currents, they always heat up during operation.

The metal sheet that helps to dissipate the additional heat from the transistor is known as *heat sink.* The heat sink avoids the undesirable thermal effect such as thermal runaway.

The ability of heat sink depends on the material used, volume, area, shape, constant between case and sink and movement of air around the sink.

The condition for Thermal Stability:

As we know, the thermal runaway may even burn and destroy the transistor, it is necessary to avoid thermal runaway.

The required condition to avoid thermal runaway is that the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated. It is given by

$$\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \qquad \text{..................(1)}$$

But we know, from thermal resistance

$$T_j - T_A = \theta P_D \qquad \text{................ (2)}$$

Differentiating equation (2) w.r.t. T_j we get

$$1 = \theta \frac{\partial P_D}{\partial T_j}$$

$$\Rightarrow \frac{\partial P_D}{\partial T_j} = \frac{1}{\theta} \qquad \text{.................. (3)}$$

Substituting equation (3) in equation (1), we get

$$\therefore \frac{\partial P_D}{\partial T_j} < \frac{1}{\theta} \qquad \text{.................. (4)}$$

This condition must be satisfied to prevent thermal runaway.

By proper design of biasing circuit it is possible to ensure that the transistor cannot runaway below a specified ambient temperature (or) even under any condition.

Let us consider voltage divider bias circuit for the analysis.

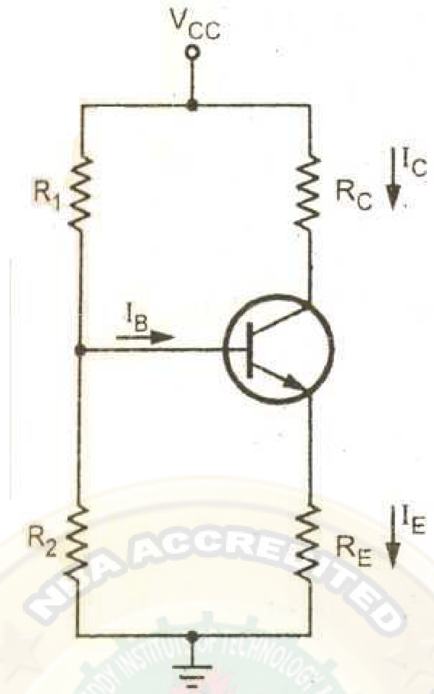


Fig. Voltage divider bias circuit.

From fig., P_C = heat generated at the collector junction.
= DC power input to the circuit – the power lost as I^2R in R_C and R_E.

If we consider $I_C \cong I_E$ we get

$$P_C = V_{CC} I_C - I_C^2 \left(R_C + R_E\right) \quad \text{………………. (6)}$$

Differentiating equation (6) w.r.t I_C we get

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C \left(R_C + R_E\right) \quad \text{………………. (7)}$$

From equation (4)

$$\frac{\partial P_C}{\partial I_C} \cdot \frac{\partial I_C}{\partial T_j} < \frac{1}{\theta} \quad \text{………………. (8)}$$

In the above equation $\frac{\partial I_C}{\partial T_j}$ can be written as

$$\frac{\partial I_C}{\partial T_j} = S \frac{\partial I_{CO}}{\partial T_j} + S' \frac{\partial V_{BE}}{\partial T_j} + S'' \frac{\partial \beta}{\partial T_j} \quad \text{……………… (9)}$$

Since junction temperature affects collector current by affecting I_{CO}, V_{BE}, and β. But as we are doing analysis for thermal runaway the affect of I_{CO} dominates. Thus we can write

$$\frac{\partial I_C}{\partial T_j} = S \frac{\partial I_{CO}}{\partial T_j} \quad \text{…………………….. (10)}$$

As the reverse saturation current for both Silicon and Germanium increases about 7 percent per ^{o}C, we can write

$$\frac{\partial I_{CO}}{\partial T_j} = 0.07 I_{CO} \qquad \text{......................... (11)}$$

Substituting equation (11) in equation (10), we get

$$\frac{\partial I_C}{\partial T_j} = S \times 0.07 I_{CO} \qquad \text{......................... (12)}$$

Substituting equations (7) and (12) in equation (8), we get

$$\left[V_{CC} - 2I_C\left(R_C + R_E\right)\right](S)\left(0.07 I_{CO}\right) < \frac{1}{\theta} \qquad \text{...................... (13)}$$

As S, I_{CO} and θ are positive; we see that the inequality in equation (13) is always satisfied provided that the quantity in the square bracket is negative.

$$\therefore V_{CC} < 2I_C\left(R_C + R_E\right)$$

$$\Rightarrow \frac{V_{CC}}{2} < I_C\left(R_C + R_E\right) \qquad \text{.................... (14)}$$

Applying KVL to the collector circuit of voltage divider bias circuit we get,

$$V_{CE} = V_{CC} - I_C\left(R_C + R_E\right) \qquad \left(\because I_C \cong I_E\right)$$

$$\therefore I_C\left(R_C + R_E\right) = V_{CC} - V_{CE}$$

Substituting the value of $I_C\left(R_C + R_E\right)$ in equation (14), we get

$$\Rightarrow \frac{V_{CC}}{2} = V_{CC} - V_{CE}$$

$$\Rightarrow V_{CC} < V_{CE} - \frac{V_{CC}}{2}$$

$$\Rightarrow V_{CE} < \frac{V_{CC}}{2}$$

Thus if $V_{CE} < \frac{V_{CC}}{2}$, the stability is ensured.

3. FIELD EFFECT TRANSISTOR

Introduction:

The filed effect transistor (abbreviated as FET) is a three terminal uni-polar semiconductor device in which current is controlled by an electric field. As current conduction is only by majority carriers, FET is said to be a uni-polar device.

Based on the construction, the FET can be classified into two types as:

a) Junction Field Effect Transistor (JFET)
b) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) or Insulated Gate Field Effect Transistor (IGFET)

Depending upon the majority carriers, JFET has been classified into two types, namely,

(1) N-Channel JFET with electrons as the majority carriers, and

(2) P-Channel JFET with holes as the majority carriers.

Construction of N-Channel JFET:

It consists of a N-type bar which is made of Silicon. Ohmic contacts (terminals), made at the two ends of the bar, are called Source and Drain.

Source (S) : This terminal is connected to the negative pole of the battery. Electronics which are the majority carriers in the N-type bar enter the bar through this terminal.

Drain (D) : This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

Gate (G) : Heavily doped P-type silicon is diffused on both sides of the N-type silicon bar by which PN junctions are formed. These layers are joined together are called Gate (G).

Channel : The region BC of the N-type bar between the depletion regions is called the Channel. Majority carriers move from the source to drain when a potential difference V_{DS} is applied between the source and drain.

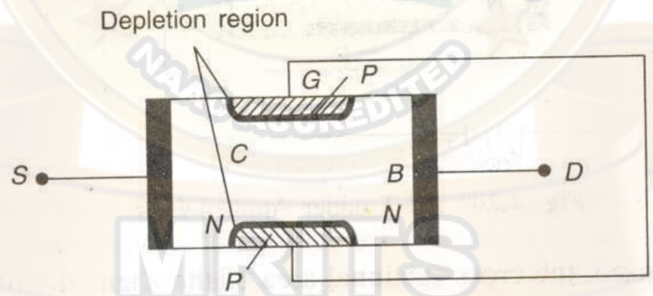
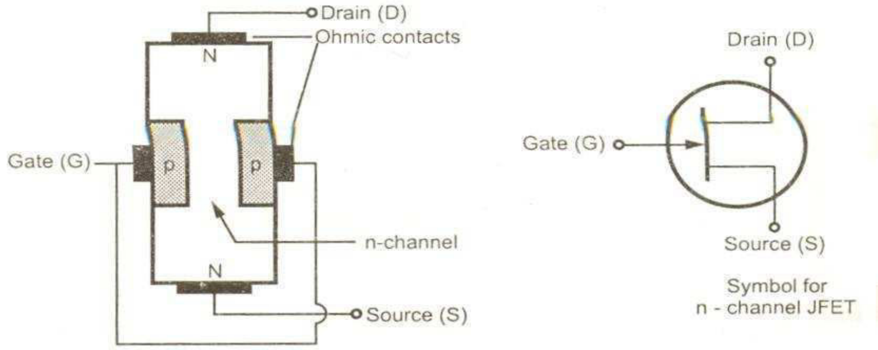


FIG. JFET construction

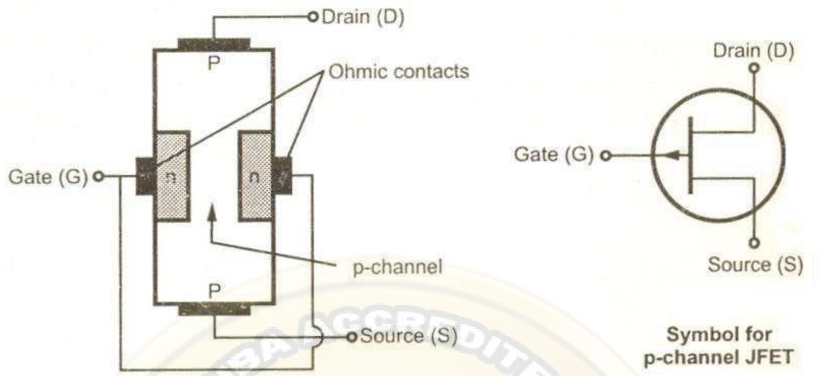
Structure and symbol of n-channel JFET:

The structure and symbol of n-channel JFET are shown in figure below.



The electrons enter the channel through the terminal called 'source' and leave through the terminal called 'drain'. The terminals taken out from heavily doped electrodes of p-type material are called 'gates'. Usually, these electrodes are connected together and only one terminal is taken out, which is called 'gate.

Structure and Symbol of P-Channel JFET:



The structure and symbol of P-Channel JFET is shown in the figure. The device could be made of P-type bar with two N-type gates as shown in the figure. Then this will be P-Channel JFET is similar; the only difference being that in N-Channel JFET the current is carried by the electrons while in P-Channel JFET, it is carried by holes.

Operation of N-Channel JFET:

The operation of N-Channel JFET can be understood with the help of figure below.

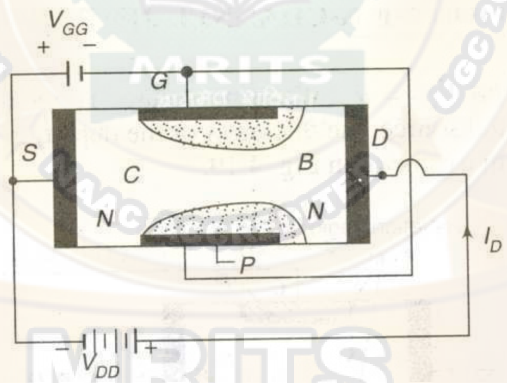
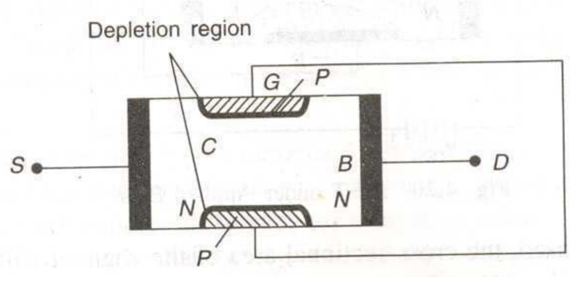


Fig. Operation of FET.

Before considering the operation, let us consider that how the depletion layers are formed. Let us first suppose that the gate has been reverse-biased by gate battery V_{GG} and the drain battery V_{DD} is not connected.

When V_{GS}=0 and V_{DS}=0:

When no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions round the P-N junction is uniform as shown in figure below.



When V_{DS}=0 and V_{GS} is decreased from zero:

In this case, the P-N junctions are reverse-biased and hence the thickness of the depletion region increases. As V_{GS} is decreased from zero, the reverse bias voltage across the P-N junction is increased and hence, the thickness of the depletion region in the channel increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cut-off. The value of V_{GS} which is required to cut-off the channel is called the cut-off voltage V_C.

When V_{GS}=0 and V_{DS} is increased from zero:

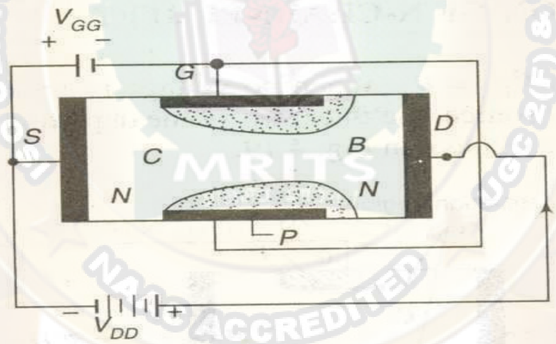
Drain is positive with respect to the source. Now the majority carriers (electrons) flow through the N-Channel from source to drain. Therefore the conventional current I_D flows from drain to source. The magnitude of the current will depend upon the following factors:

1. The conductivity of the channel.
2. The length of the channel.
3. The cross sectional area 'A' of the channel.
4. The magnitude of the applied voltage V_{DS}.

Thus the channel acts as a resistor of resistance 'R' is given by, $R = \frac{\rho L}{A}$

$$I_D = \frac{V_{DS}}{R} = \frac{AV_{DS}}{\rho L}$$

Where 'ρ' is the resistivity of the channel. As V_{DS} increases, the reverse voltage across the P-N junction increase and hence the thickness of the depletion region also increases. Therefore, the channel is wedge shaped as shown in fig. below.



As V_{DS} is increase, at a certain value V_P of V_{DS}, the cross sectional area of the channel becomes minimum. At this voltage, the channel is said to be pinched off and the drain voltage V_P is called the pinch-off voltage.

As a result of the decreasing cross-section of the channel with the increase of V_{DS}, the following results are obtained.

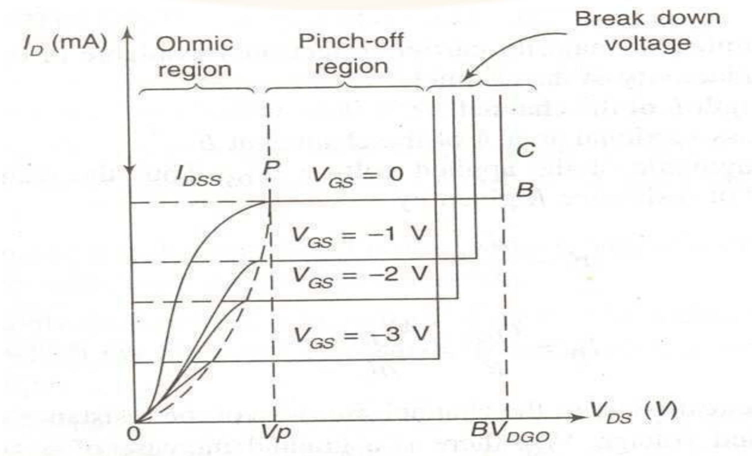


Fig. Drain characteristics.

i) As V_{DS} is increased from zero, I_D increases linearly along OP, this region from V_{DS}=0 to $V_{DS}=V_P$ is called the ohmic region. In this region, the FET acts as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

ii) When $V_{DS}=V_P$, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off (or) saturation region increases. Hence, there is no further increase of I_D.

iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the Avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain. The drain voltage at which the breakdown occurs is denoted by BV_{DGO}.

When V_{GS} is negative and V_{DS} is increased:

When the gate is maintained at a negative voltage less than the negative cut-off voltage, the reverse voltage across the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for V_{GS}=0, but the values of V_P and BV_{DGO} are lower.

The drain current I_D is controlled by the electric field that extends into the channel due to reverse biased voltage applied to the gate, hence, this device has been given the name Field Effect Transistor.

Characteristics Parameters of the JFET:

In a JFET, the drain current I_D depends upon the drain voltage V_{DS} and the gate voltage V_{GS}. Any one of these variables may be fixed and the relation between the other two is determined. These relations are determined by the three parameters which defined below.

1) Mutual Conductance (or) transconductance, g_m:

It is the slope of the transfer characteristic curves, and is defined by,

$$g_m = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}}$$, V_{DS} held constant

2) Drain resistance, r_d :

It is the reciprocal of the slope of the drain characteristics and is defined as,

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}$$, V_{GS} held constant

The reciprocal of r_d is called the drain conductance. It is denoted g_d (or) g_m.

3) Amplification Factor, μ:

It is defined by,

$$\mu = -\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)_{I_D} = -\frac{\Delta V_{DS}}{\Delta V_{GS}}$$, I_D held constant.

Relationship among FET parameters:

As I_D on V_{DS} and V_{GS}, the functional equation can be expressed as

$I_D = f(V_{DS}, V_{GS})$

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS}$$

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

If I_D is constant, then $\frac{\Delta I_D}{\Delta V_{GS}} = 0$

Therefore, we have $$0 = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

$$\Rightarrow 0 = \left(\frac{1}{r_d}\right)(-\mu) + g_m$$

Hence, $\mu = r_d \times g_m$

$$\Rightarrow \mu = g_m r_d$$

Expression for Saturation Drain Current:

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

I_{DS} = saturation Drain Current.
I_{DSS} = the value of I_{DS} when V_{GS}=0.
V_P = the pinch-off voltage.

Comparison of JEFT and BJT

1. FET operation depends only on the flow of majority carriers – holes for p-channel FET's and electrons for N-channel FET's. Therefore, they are called Uni-Polar devices. Bipolar transistor (BJT) operation depends on both minority and majority current devices.
2. As FET has no junctions and the conduction is through an N-type (or) P-type semiconductor material, FET is less noisy than BJT.
3. As the input circuit of FET is reverse biased, FET exhibits a much higher input impedance (in the order of 100MΩ) and lower output impedance and there will be a high degree of isolation between input and output. So, FET can acts as an excellent buffer amplifier but the BJT has low input impedance because its input circuit is forwards biased.
4. FET is a voltage controlled device, i.e., voltage at the input terminal controls the output current, whereas BJT is a current controlled device, i.e., the input current controls the output current.
5. FET's are much easier to fabricate and are particularly suitable for IC's because they occupy less space than BJT's.
6. The performance of BJT is degraded by neutron radiation because of the reduction in minority-carrier life time, whereas FET can tolerate a much higher level of radiation since they do not rely on minority carriers for their operation.
7. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature co-efficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature co-efficient at high current levels which leads to thermal breakdown.

8. Since FET does not suffer from minority carrier storage effects, it has higher switching speeds and cut-off frequencies. BJT suffers from minority carrier storage effects and therefore has lower switching speed and cut-off frequencies.
9. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
10. BJT�टs are cheaper to produce than FET's.

Comparison of N-channel with P-Channel FET's

1. In an N-channel JFET the current carriers are electrons, whereas the current carriers are holes in a P-channel JFET.
2. Mobility of electrons is large in N-channel JFET, mobility of holes is poor in P-channel JFET.
3. The input noise is less in N-channel JFET than that of P-channel JFET.
4. The transconductance is larger in N-channel JFET than that of P-channel JFET.

Applications of JFET

1. FET is used as a buffer in measuring instruments, receivers since it has high input impedance and low output impedance.
2. FET's are used in Radio Frequency amplifiers in FM (Frequency Mode) tuners and communication equipment for the low noise level.
3. Since the input capacitance is low, FET's are used in cascade amplifiers in measuring and test equipments.
4. Since the device is voltage controlled, it is used as voltage variable resistor in operational amplifiers and tone controls
5. FET's are used in mixer circuits in FM and TV receivers, and communication equipments because inter modulation distortion is low.
6. It is used in oscillator circuits because frequency drift is low.
7. As the coupling capacitor is small, FET's are used in low frequency amplifiers in hearing aids and inductive transducers.
8. FET's are used in digital circuits in computers, LSD and a memory circuit because of it is small size.

Biasing of FET:

- The Parameters of FET is temperature dependent .When temperature increases drain resistance also increases, thus reducing the drain current.
- Unlike BJTs, thermal runaway does not occur with FETs
- However, the wide differences in maximum and minimum transfer characteristics make I_D levels unpredictable with simple fixed-gate bias voltage.

Different biasing circuits of FET are

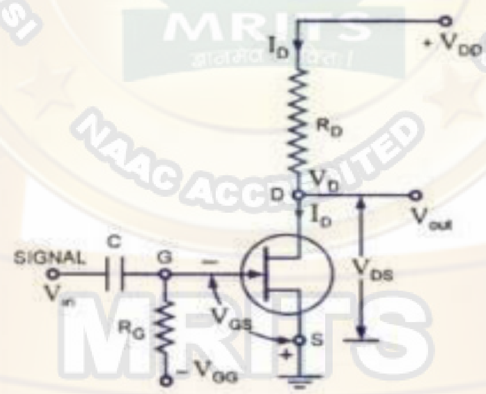
A. Fixed bias circuits

B. Self bias circuits

C. Voltage bias circuits

A. Fixed bias circuits

DC bias of a FET device needs setting of gate-source voltage V_{GS} to give desired drain current I_D . For a JFET drain current is limited by the saturation current I_{DS}. Since the FET has such a high input impedance that no gate current flows and the dc voltage of the gate set by a voltage divider or a fixed battery voltage is not affected or loaded by the FET.



Fixed Biasing Circuit For JFET

Fixed dc bias is obtained using a battery V_{QG}. This battery ensures that the gate is always negative with respect to source and no current flows through resistor R_G and gate terminal that is I_G =0. The battery provides a voltage V_{GS} to bias the N-channel JFET, but no resulting current is drawn from the battery V_{GG}. Resistor R_G is included to allow any ac signal applied through capacitor C to develop across R_G. While any ac signal will develop across R_G, the dc voltage drop across R_G is equal to I_G R_G*i.e.* 0 volt.

Calculate V_{GS}

For DC analysis I_G =0., applying KVL to the input circuits

$V_{GS}+ V_{GG}=0$

$V_{GS}= - V_{GG}$

As V_{GS} is a fixed dc supply, hence the name fixed bias circuit

Calculate I_{DQ}

$I_{DQ}=IDss(1- V_{GS}/V_{Gp})^2$

Calculate V_{DS}

This current I_{DQ} then causes a voltage drop across the drain resistor R_D and is given as

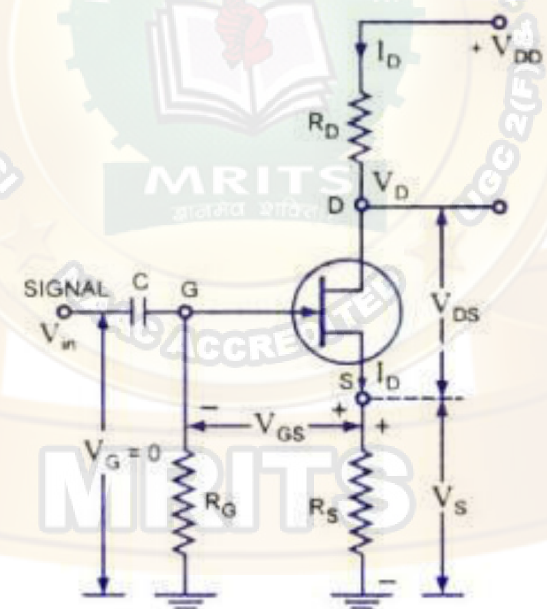
$V_{DSQ} = V_{DD} – I_D R_D$

Disadvantage

The fixed bias circuit of FET requires two power supplies.

B. <u>Self-Bias circuits</u>

Self-Bias circuits is the most common method for biasing a JFET. Self-bias circuit for N-channel JFET is shown in figure



Self-Bias Circuit For N-Channel JFET

The gate source junction of JFET must be always in reverse biased condition .No gate current flows through the reverse-biased gate-source, the gate current $I_G = 0$ and,

therefore, $v_G = i_G R_G = 0$

1)The gate-source voltage is then

With a drain current I_D the voltage at the S is $V_s= I_DR_s$

$V_{GS} = V_G - V_s = 0 – I_D R_S = – I_D R_S$

So voltage drop across resistance R_s provides the biasing voltage V_{Gg} and no external source is required for biasing and this is the reason that it is called self-biasing.

2)Calculate I_{DQ}

$I_D = I_{DSS}(1 - V_{GS}/ V_P)^2$

Substituting the value of VGS

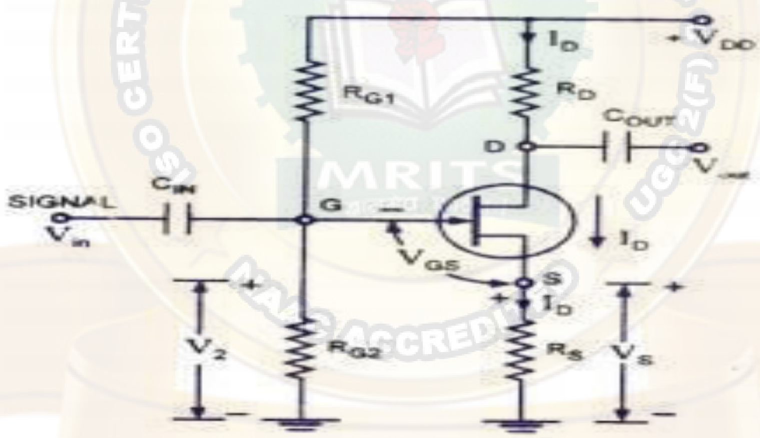
$I_D = I_{DSS}\ (1 + I_D R_S\ /\ V_P)^2$

3)The operating point *(*that is zero signal I_D and V_{DS}) can easily be determined from equation given below :

$V_{DS} = V_{DD} – I_D(R_D + R_S)$

Self biasing of a JFET stabilizes its quiescent operating point against any change in its parameters like transconductance. Any increase in voltage drop across R_S, therefore, gate-source voltage, V_{GS} becomes more negative and thus increase in drain current is reduced.

C.Voltage -Divider Bias circuits



Potential-Divider Bias Circuit
For N-Channel JFET

The resistors R_{GI} and R_{G2} form a potential divider across drain supply V_{DD}. The voltage V_2 across R_{G2} provides the necessary bias. The additional gate resistor R_{GI} from gate to supply voltage facilitates in larger adjustment of the dc bias point and permits use of larger valued R_S.

The coupling capacitors are assumed to be open circuit for DC analysis

1) The gate is reverse biased so that $I_G = 0$ and gate voltage

$V_G = V_2 = (V_{DD}/R_{G1} + R_{G2}) * R_{G2}$

2) Applying KVL to the input circuit we get

$V_{GS} = \mathbf{V}_G – V_S = V_G - I_D R_S$

3) $I_{DQ} = I_{DSS}(1 - V_{GS}/ V_P)^2$

4) $V_{DS} = V_{DD} – I_D (R_D + R_S)$

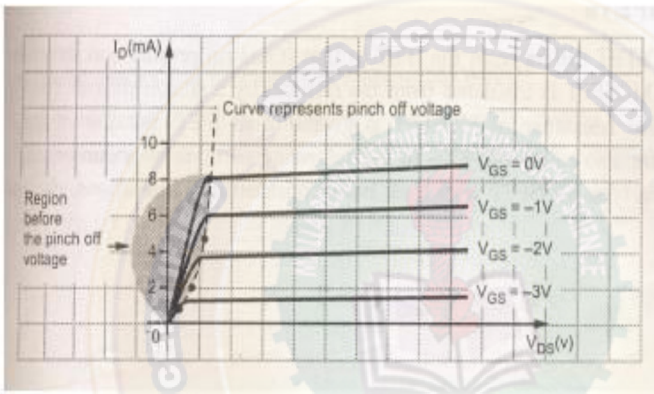
The operating point of a JFET amplifier using the Voltage -Divider Bias is determined by

$I_{DQ}= I_{DSS}(1- V_{GS}/ V_P)^2$

$V_{DSQ} = V_{DD} – I_D (R_D + R_S)$

$V_{GSQ} = V_G – I_D R_S$

FET as a Voltage Variable Resistor



In this characteristics we can see that in the region before pinch off voltage, drain characteristics are linear, i.e. FET operation is linear. In this region the FET is useful as a voltage controlled resistor,i.e. the drain to source resistance is controlled by the bias voltage VGS.(In this region only FET behaves like an ordinary resistor This resistances can be varied by VGS) .The operation of FET in the region is useful in most linear applications of FET.In such an application the FET is also referred to as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

The drain to source conductance (rd)

$g_d=\frac{Id}{Vds}$ for small values of VDS which may also be expressed as

$g_d=g_{d0}(1-(\frac{Vgs}{Vp})^{1/2})$

Where g_{d0} is the value of drain conductance

When the variation of the rd with VGS can be closely approximated by the expression

$rd=(\frac{r0}{1-KVgs})$ Where ro = drain resistance at zero gate bias.K = a constant, dependent upon FET type.

SPECIAL PURPOSE DEVICES

Zener Diode:

Zener Diode is a reverse-biased heavily-doped PN junction diode which operates in the breakdown region. The reverse breakdown of a PN- junction may occur either due to Zener effect or avalanche effect. Zener effect dominates at reverse voltages less than 5 volt whereas avalanche effect dominates above 5 V. Hence, first one should be called Zener diode. But for simplicity, both types are called Zener Diodes. The breakdown voltage of a Zener diode can be set by controlling the doping level. For Zener diodes, silicon is preferred to Ge because of its high temperature and current capability. This post includes explanation of operation of Zener diode and V-I Characteristics of Zener Diode.

Operation of Zener Diode:

- Zener Diodes are normally used only in the reverse bias direction.
- It means that the anode must be connected to the negative side of the voltage source and the cathode must be connected to the positive side.
- A main difference between Zener diodes and regular silicon diodes is the way they are used in the circuits.
- It is primarily used to regulate the circuit voltage as it has constant Vz.
- A large change in IR will cause only a small change in Vz. It means that a zener diode can be used as an alternate current path. The constant Vz developed across the diode can then be applied to a load.
- Thus the load voltage remains at constant by altering the current flow through the Zener diode.

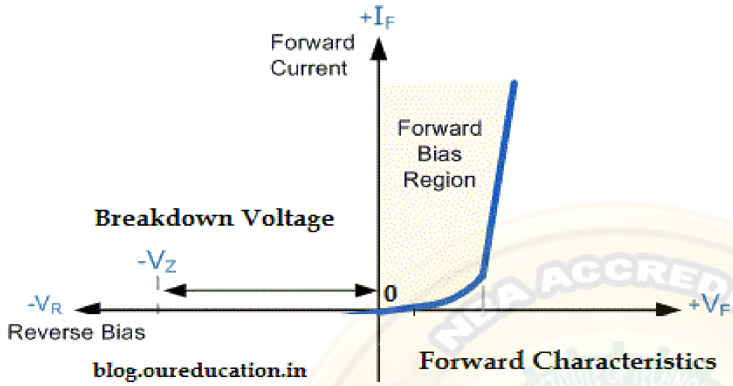
The V-I Characteristics of a Zener Diode can be divided into two parts

(i) Forward Characteristics

(ii) Reverse Characteristics

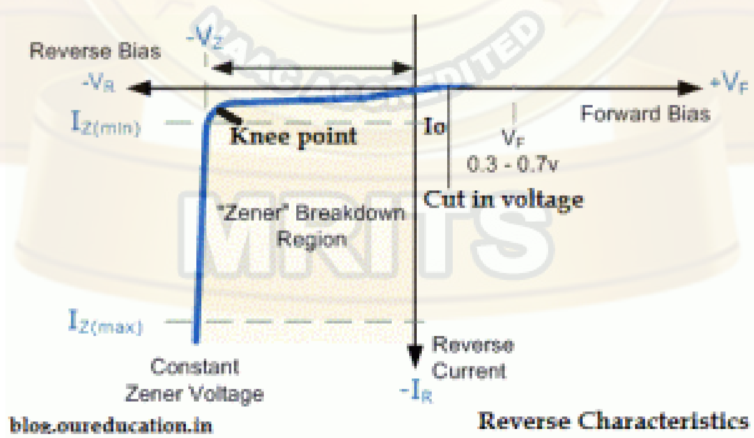
Forward Characteristics

The forward characteristics of a Zener diode is shown in figure. It is almost identical to the forward characteristics of a P-N junction diode.



Reverse Characteristics

As we increase the reverse voltage, initially a small reverse saturation current Io. Which is in A, will follow. This current flows due to the thermally generated minority carriers. At a certain value of reverse voltage, the reverse current will increase suddenly and sharply . This is an indication that the breakdown has occurred. This breakdown voltage is called as Zener breakdown voltage or Zener voltage and it is denoted by V_z.

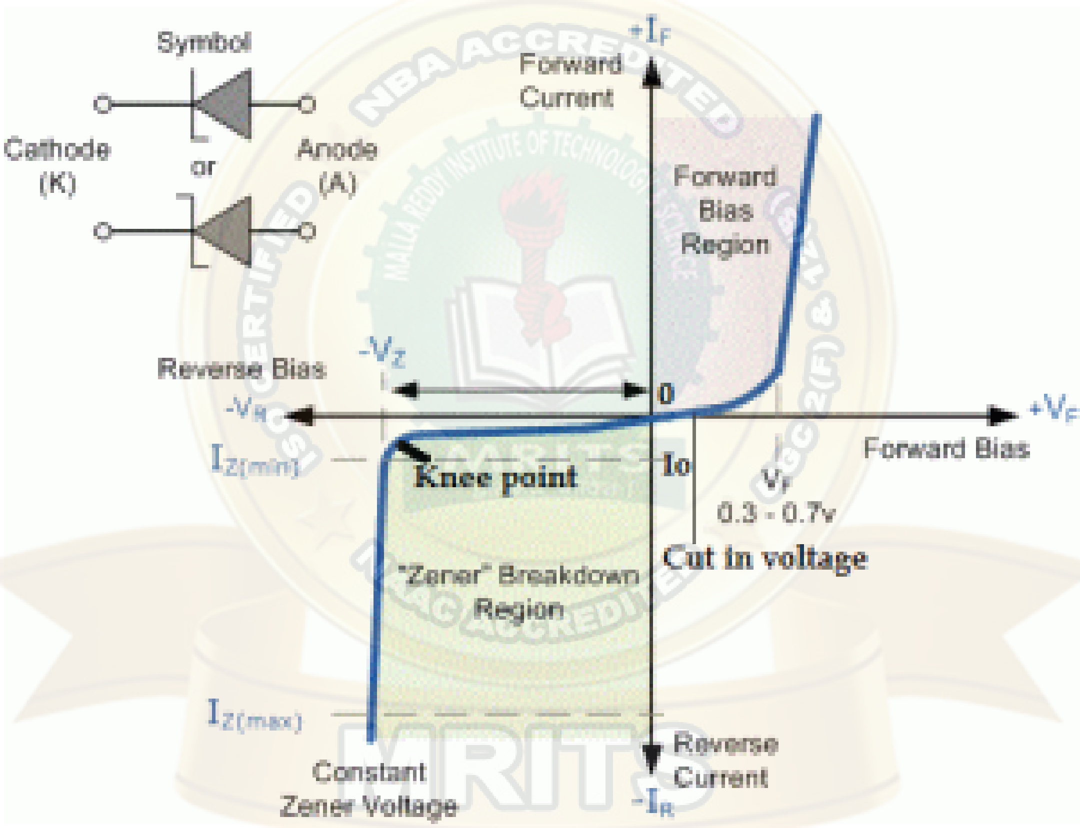


Reverse Characteristics of Zener Diode

The value of V_z can be precisely controlled by controlling the doping levels of P and N regions at the time of manufacturing a Zener diode. After breakdown has occurred. The voltage across Zener diode remains constant equal to V_z. Any increase in the source voltage will result in the increase in reverse Zener current. The Zener current after the reverse breakdown must be controlled by connecting a resistor R as shown in figure. This is essential to avoid any damage to the device due to excessive heating.

Zener Region and its importance

Reverse breakdown of the zener diode operates in a region called zener region, as shown in figure. In this region the voltage across zener diode remains constant but current changes depending on the supply voltage. zener diode is operated in this region when it is being used as a voltage regulator. The complete v-i characteristics of zener diode is as shown in figure



V-I Characteristics of Zener Diode

BREAKDOWN MECHANISMS IN DIODES:

The avalanche breakdown occurs because of the ionisation of electrons(reverse saturation current) and hole pairs whereas the Zener breakdown occurs because of **heavy doping**. These are explained below in details.

Avalanche Breakdown:

The mechanism of avalanche breakdown occurs because of the reverse saturation current. The P-type and N-type material together forms the PN-junction. The depletion region develops at the junction where the P and N-type material contact.

The P and N-type materials of the PN junction are not perfect, and they have some impurities in it, i.e., the p-type material has some electrons, and the N-type material has some hole in it. The width of the depletion region varies. Their width depends on the bias applied to the terminal of the P and N region.

The reverse bias increases the electrical field across the depletion region. When the high electric field exists across the depletion, the velocity of minority charge carrier crossing the depletion region increases . These carriers collide with the atoms of the crystal. Because of the violent collision, the charge carrier takes out the electrons from the atom.

The collision increases the electron-hole pair. As the electron-hole induces in the high electric field, they are quickly separated and collide with the other atoms of the crystals. The process is continuous, and the electric field becomes so much higher then the reverse current starts flowing in the PN junction. The process is known as the **Avalanche breakdown**. After the breakdown, the junction cannot regain its original position because the diode is completely burnt off.

Zener Breakdown:

The PN junction is formed by the combination of the p-type and the n-type semiconductor material. The combination of the P-type and N-type regions creates the depletion region.

The width of the depletion region depends on the doping of the P and N-type semiconductor material. If the material is heavily doped, the width of the depletion region becomes very thin.

The phenomenon of the Zener breakdown occurs in the very thin depletion region. The thin depletion region has more numbers of free electrons. The reverse bias applies across the PN junction develops the electric field intensity across the depletion region. The strength of the electric field intensity becomes very high.

The electric field intensity increases the kinetic energy of the free charge carriers. Thereby the carriers start jumping from one region to another. These energetic charge carriers collide with the atoms of the p-type and n-type material and produce the electron-hole pairs.

The reverse current starts flowing in the junction because of which depletion region entirely vanishes. This process is known as the Zener breakdown.

Applications of zener Diode are as follows:

Zener diodes have a large number of application. few of them are

(i) Zener diode is used as a voltage regulator.

(ii) Zener diode is used as a peak clipper in wave shaping circuits.

(iii) Zener diode is used as a fixed reference voltage in transistor biasing circuits.

(iv) Zener diode is used for meter protection against damage from accidental application of excessive voltages

Zener Diode as Voltage Regulators:

The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum $I_{Z(min)}$ value in the reverse breakdown region. It permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above a certain value - the breakdown voltage known as the Zener voltage. The Zener diode specially made to have a reverse voltage breakdown at a specific voltage. Its characteristics are otherwise very similar to common diodes. In breakdown the voltage across the Zener diode is close to constant over a wide range of currents thus making it useful as a shunt voltage regulator.

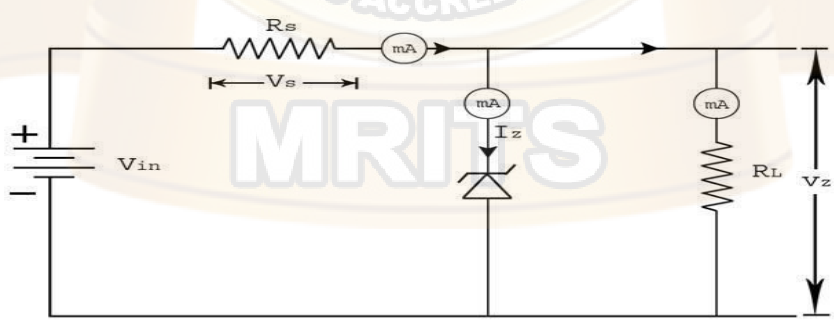


Fig 3**: Zener diode shunt regulator**

The purpose of a voltage regulator is to maintain a constant voltage across a load regardless of variations in the applied input voltage and variations in the load current. A typical Zener diode shunt regulator is shown in Figure 3. The resistor is selected so that when the input voltage is at $V_{IN(min)}$ and the load current is at $I_{L(max)}$ that the current through the Zener diode is at least $I_{z(min)}$. Then for all other combinations of input voltage and load current the Zener diode conducts the excess current thus maintaining a constant voltage across the load. The Zener conducts the least current when the load current is the highest and it conducts the most current when the load current is the lowest.

If there is no load resistance, shunt regulators can be used to dissipate total power through the series resistance and the Zener diode. Shunt regulators have an inherent current limiting advantage under load fault conditions because the series resistor limits excess current.

A zener diode of break down voltage V_z is reverse connected to an input voltage source V_i across a load resistance R_L and a series resistor R_S. The voltage across the zener will remain steady at its break down voltage V_Z for all the values of zener current I_Z as long as the current remains in the break down region. Hence a regulated DC output voltage $V_0 = V_Z$ is obtained across RL, whenever the input voltage remains within a minimum and maximum voltage.

Basically there are two type of regulations such as:

a) Line Regulation

In this type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value.Percentage of line regulation can be calculated by = $\frac{\Delta V_0}{\Delta V_{IN}} * 100$

where V_0 is the output voltage and V_{IN} is the input voltage and ΔV_0 is the change in output voltage for a particular change in input voltage ΔV_{IN}.

b) Load Regulation

In this type of regulation, input voltage is fixed and the load resistance is varying. Output volt remains same, as long as the load resistance is maintained above a minimum value.

Percentage of load regulation = $\left[\frac{V_{NL} - V_{FL}}{V_{NL}}\right] * 100$

where V_{NL} is the null load resistor voltage (ie. remove the load resistance and measure the voltage across the Zener Diode) and V_{FL} is the full load resistor voltage

UNIJUNCTION TRANSISTOR:

Uni Junction Transistor (UJT) is a three terminal semi conductor switching device. As it has only one PN junction and three leads, it is commonly called as Uni Junction Transistor.

The three terminals are: Emitter (E), Base1 (B1) and Base2 (B2).

Construction and Symbol:

The basic structure and symbol of UJT is shown in figure below.

It consists of a lightly doped n-type silicon bar with a heavily doped p-type material alloyed to its one side closer to B2 for producing single PN junction.

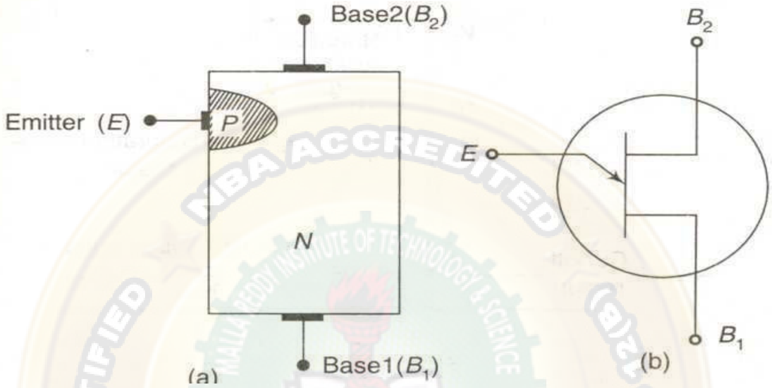


Fig. UJT (a) Basic structure (b) Circuit symbol

Here the emitter leg is drawn at an angle to the vertical and the arrow indicates the direction of the conventional current.

Operation of UJT:

The inter base resistance between B2 and B1 of the silicon bar is, $R_{BB}=R_{B1}+R_{B2}$.

With emitter terminal open, if voltage V_{BB} is applied between the two bases, a voltage gradient is established along the n-type bar.

The voltage drop across R_{B1} is given by $V_1=\eta V_{BB}$, where the intrinsic stand-off ratio $\eta=\frac{R_{B1}}{R_{B1}+R_{B2}}$. The typical value of η ranges from 0.56 to 0.75.

This voltage V_1 reverse biases the PN-junction and emitter current is cut-off. But a small leakage current flows from B2 to emitter due to minority carriers. The equivalent circuit of UJT is shown in figure below.

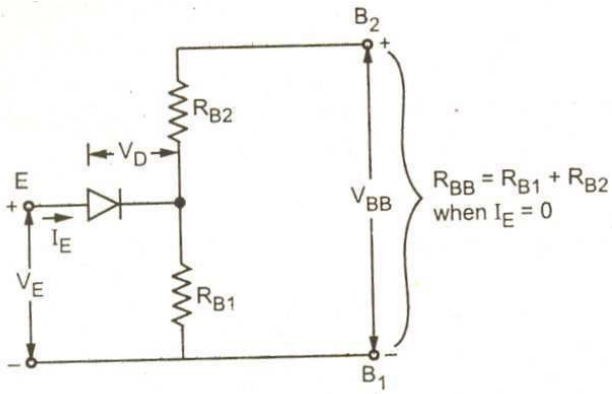


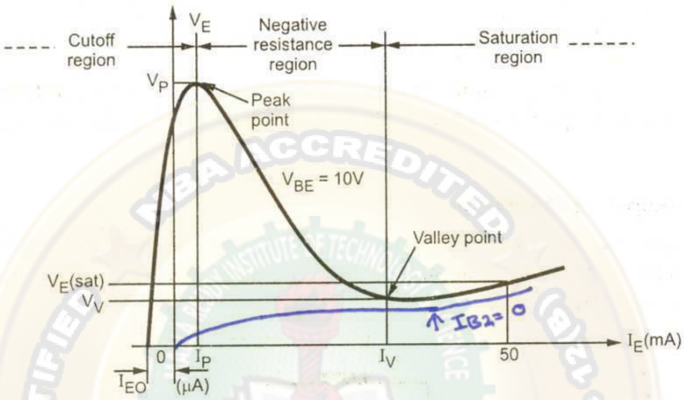
Fig. UJT equivalent circuit.

If a negative voltage is applied to the emitter, PN-junction remains reverse biased and the emitter current is cut-of. The device is now in the 'OFF' state.

If a positive voltage V_E is applied to the emitter, the PN-junction will remain reverse biased so long as V_E is less than V_1. If V_E exceeds V_1 by the cut-in voltage vγ, the diode becomes forward biased. Under this condition, holes are injected into n-type bar. These holes are repelled by the terminal B2 and are attracted by the terminal B1. Accumulations of holes in E to B1 region reduce the resistance in this section and hence emitter current I_E is increased and is limited by V_E. The device is now in the 'ON' state.

Characteristics of UJT:

Figure below shows the input characteristics of UJT.



Here, up to the peak point P, the diode is reverse biased and hence, the region to the left of the peak point is called cut-off region.

At P, the peak voltage $V_P = \eta V_{BB} + V_\gamma$, the diode starts conducting and holes are injected into n-layer. Hence, resistance decreases thereby decreasing V_E for the increase in I_E. SO there is a negative resistance region from peak point P to valley point V.

After the valley point, the device is driven into saturation and behaves like a conventional forward biased PN-junction diode. The region to the right of the valley point is called saturation region. In the valley point, the resistance is changes from negative to positive. The resistance remains positive in the saturation region.

Due to the negative resistance property, a UJT can be employed in a variety of applications, viz., a saw-tooth wave generator, pulse generator, switching, timing and phase control circuits.

UJT Relaxation Oscillator:

The Relaxation oscillator using UJT which is meant for generating saw-tooth waveform is shown in figure below:

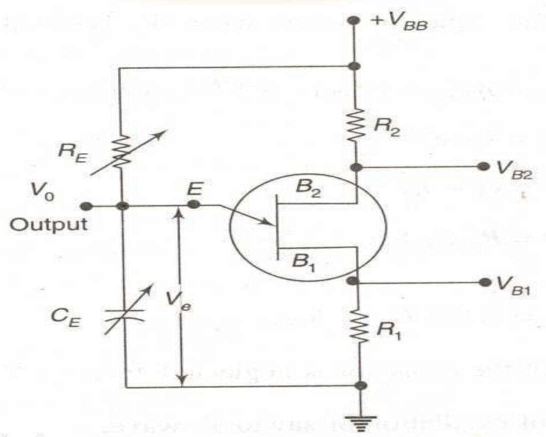
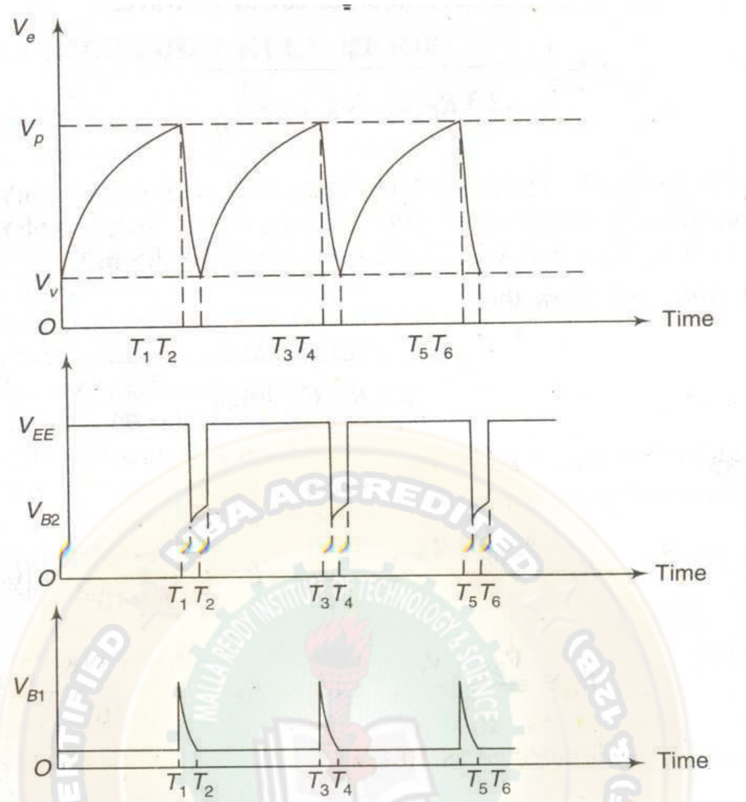


Fig: UJT Relaxation Oscillator.

It consists of a UJT and a capacitor C_E which is charged through R_E as the supply voltage V_{BB} is switched ON.



The voltage across the capacitor increases exponentially and when the capacitor voltage reach the peak point voltage V_P, the UJT starts conducting and the capacitor voltage is discharged rapidly through EB1 and R1.

After the peak point voltage of UJT is reached, it provides negative resistance to the discharge path which is useful in the working of the relaxation oscillator. As the capacitor voltage reaches zero, the device then cuts off and capacitor C_E starts to charge again. This cycle is repeated continuously generating a saw-tooth waveform across C_E.

The inclusion of external resistors R2 and R1 in series with B2 and B1 provides spike waveforms. When the UJT fires, the sudden surge of current through B1 causes drop across R1, which provides positive going spikes.

Also, at the time of firing, fall of V_{EB1} causes I_2 to increase rapidly which generates negative going spikes across R_2. By changing the values of capacitance C_E (or) resistance R_E, frequency of the output waveform can be changed as desired, since these values control the time constant R_EC_E of the capacitor changing circuit.

Frequency of oscillations:

The time period and hence the frequency of the saw-tooth wave can be calculated as follows. Assuming that the capacitor is initially uncharged, the voltage V_C across the capacitor prior to breakdown is given by

$$V_C = V_{BB}\left(1 - e^{-t/R_E C_E}\right)$$

Where R_EC_E = charging time constant of resistor-capacitor circuit, and t= time from the commencement of the waveform. The discharge of the capacitor occurs when V_C is equal to the peak-point voltage V_P, i.e,

$$V_P = \eta V_{BB} = V_{BB}\left(1 - e^{-t/R_E C_E}\right)$$

$$\Rightarrow \eta = 1 - e^{-t/R_E C_E}$$

$$e^{-t/R_E C_E} = 1 - \eta$$

$$\therefore t = R_E C_E \log_e\left(\frac{1}{1-\eta}\right)$$

$$= 2.303 R_E C_E \log_{10}\left(\frac{1}{1-\eta}\right)$$

If the discharge time of the capacitor is neglected, then t=T, the period of the wave. Therefore, frequency of oscillations of saw-tooth wave,

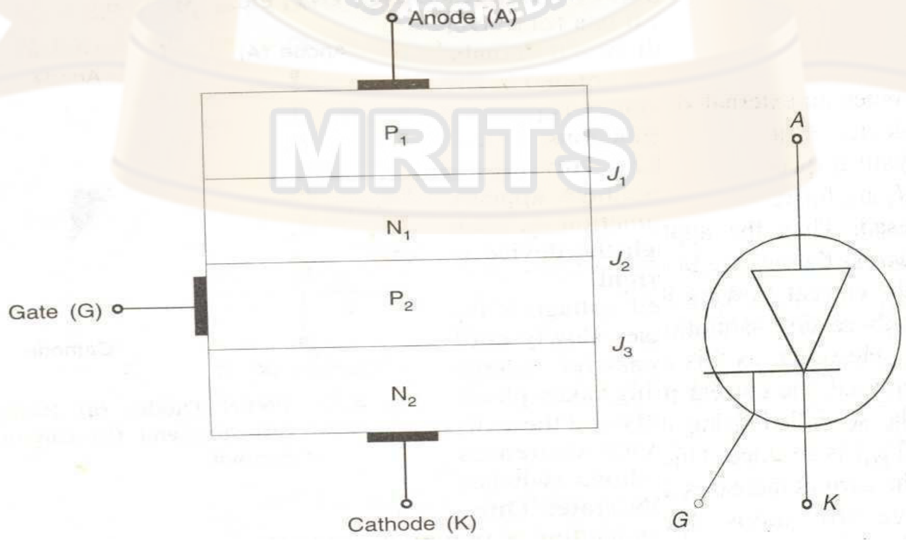
$$f = \frac{1}{T} = \frac{1}{2.3 R_E C_E \log_{10}\left(\frac{1}{1-\eta}\right)}$$

SCR (SILICON CONTROLLED RECTIFIER)

The basic structure and circuit symbol of SCR is shown in figure below.

It is a four layer three terminal device in which the end p-layer acts as anode, the end n-layer acts as anode, the end n-layer acts as cathode and p-layer nearer to cathode acts as gate.

As leakage current in silicon is very small compared to germanium, SCR's are made of silicon and not germanium.



(a) Basic Structure (b) Circuit symbol

Fig, Basic structure and circuit symbol of SCR.

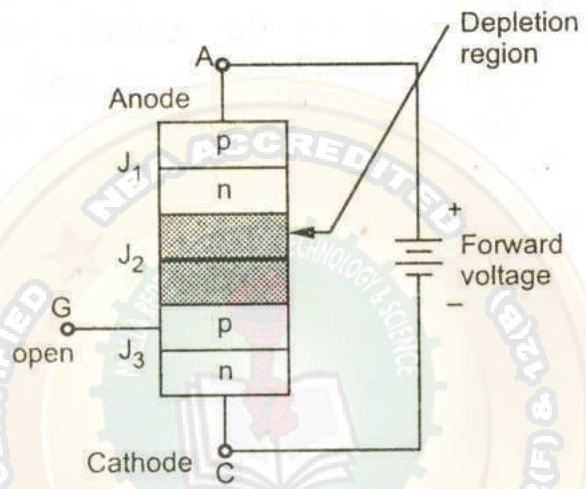
Operation of SCR:

The operation of SCR is divided into two categories,

i) When gate is open:

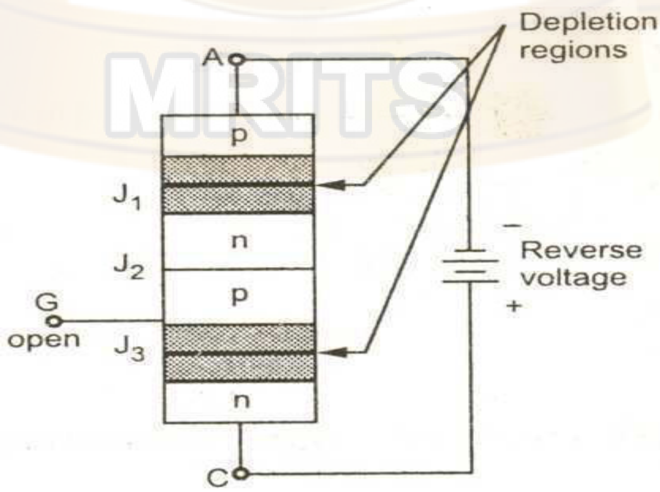
Consider that the anode is positive with respect to cathode and gate is open.

The junctions J_1 and J_3 are forward biased and junctions J_2 is reverse biased. There is depletion region around J_2 and only leakage current flows which is negligibly small. Practically the SCR is said to be 'OFF'. This is called forward blocking state of SCR and voltage applied to anode and cathode with anode positive is called *forward voltage.* This is shown in figure (a) below.



(a) J_1, J_3 Forward biased.
J_2 Reverse biased.

With gate open, if cathode is made positive with respect to anode, the junctions J_1, J_3 become reverse biased and J_2 forward biased. Still the current flowing is leakage current, which can be neglected as it is very small. The voltage applied to make cathode positive is called reverse voltage and SCR is said to be in reverse blocking state. This is shown in the figure (b) below.



(a) J_1, J_3 Reverse biased.
J_2 Forward biased.
Fig. Operation of SCR when gate is open (a), (b).

2. When gate is closed:

Consider that the voltage is applied between gate and cathode when the SCR is in forward blocking state. The gate is made positive with respect to the cathode. The electrons from n-type cathode, which are majority in number, cross the junction J_3 to reach to positive of battery.

While holes from p-type move towards the negative of battery. This constitutes the gate current. This current increases the anode current as some of the electrons cross junction J_2. As anode current increases, more electrons cross the junction J_2 and the anode current further increases. Due to regenerative action, within short time, the junction J_2 breaks and SCR conducts heavily.

The connections are shown in the figure. The resistance R is required to limit the current. Once the SCR conducts, the gate loses its control.

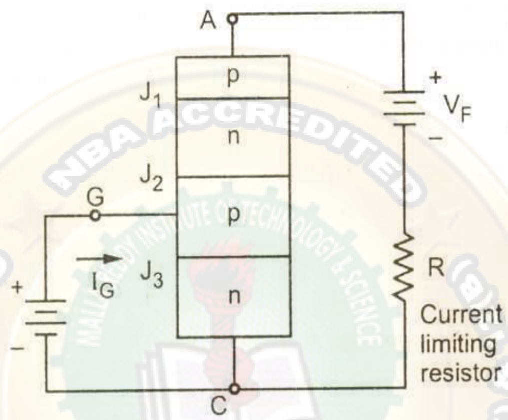


Fig. Operation of SCR when gate is closed.

Characteristics of SCR:

The characteristics are divided into two sections:

i) Forward characteristics
ii) Reverse characteristics

i) Forward characteristics:

It shows a forward blocking region, when I_G=0. It also shows that when forward voltage increases up to V_{BO}, the SCR turns ON and high current results.

It also shows that, if gate bias is used then as gate current increases, less voltage is required to turn ON the SCR.

If the forward current falls below the level of the holding current I_H, then depletion region begins to develop around J_2 and device goes into the forward blocking region.

When SCR is turned on from OFF state, the resulting forward current is called *latching current* I_L. The latching current is slightly higher than the holding current

ii) Reverse characteristics:

If the anode to cathode voltage is reversed, then the device enters into the reverse blocking region. The current is negligibly small and practically neglected.

If the reverse voltage is increases, similar to the diode, at a particular value avalanche breakdown occurs and a large current flows through the device. This is called reverse breakdown and the voltage at which this happens is called reverse breakdown voltage

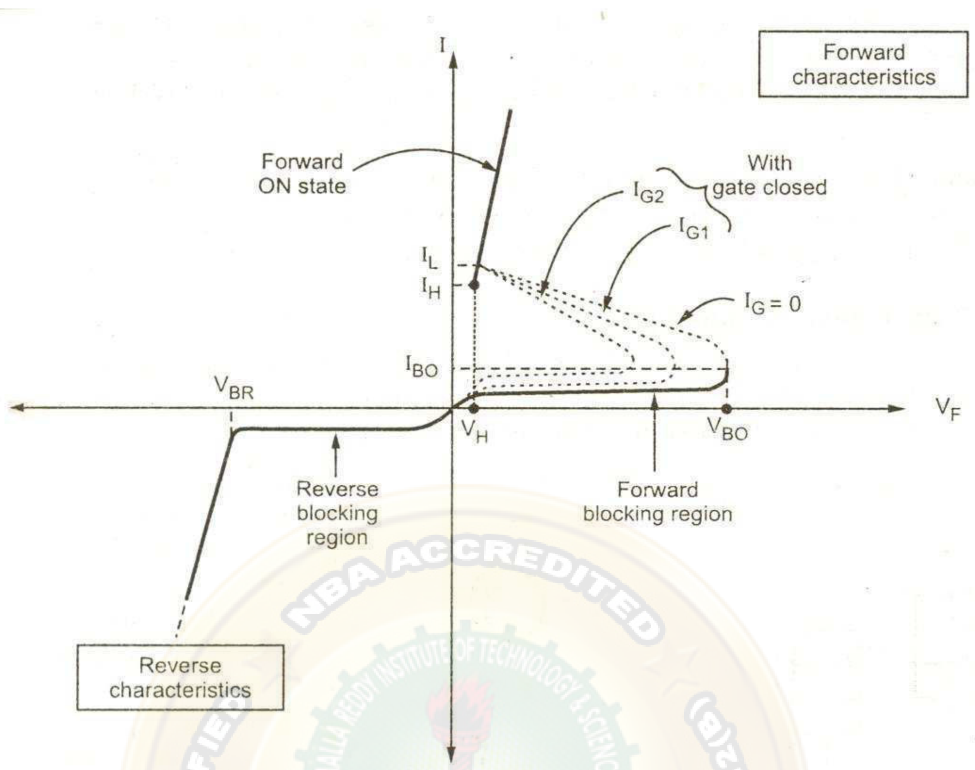
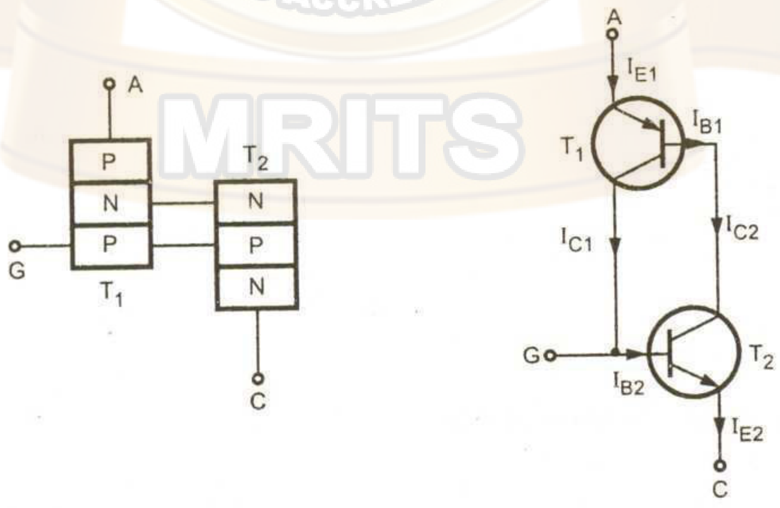


Fig. Characteristics of SCR.

Two Transistor Analogy:

The easiest way to understand how SCR works it ot visualize it separately into two halves, as shown in the figure. The left half is a p-n-p transistor and right half is n-p-n transistor. This is also called two transistor model of SCR.

The collector current of T_1 becomes base current of T_2 and collector current of T_2 becomes base current of T_1.



Fig, Two transistor model of SCR.

Mathematical Analysis:

Let I_{C1} and I_{C2} are collector currents, I_{E1} and I_{E2} are emitter currents while I_{B1} and I_{B2} are base currents of transistors T_1 and T_2.

Let both the transistors are operating in active region.

From transistor analysis we can write,

$$I_{C1} = \alpha IE_1 + I_{CO1} \text{ and } I_{C2} = \alpha IE_2 + I_{CO2}$$

Where I_{CO} = Reverse current (or) leakage current.

And $\alpha = \dfrac{\beta}{1+\beta}$

Now, $I_{E2} = I_{C2} + I_{B2}$

I_A = Anode current = I_{E1}
I_K = Cathode current = I_{E2}
I_G = Gate current

Now, $I_K = I_A + I_G$

$$\therefore I_{E2} = I_A + I_G = I_{C2} + I_{B2}$$

But $I_{B2} = I_{C1} + I_G$

$$\therefore I_A + I_G = I_{C2} + I_{C1} + I_G$$

Substituting I_{C1} and I_{C2},

$$\therefore I_A = \alpha_1 IE_1 + I_{CO1} + \alpha_2 IE_2 + I_{CO2}$$

$$\therefore I_A = \alpha_2 \left(I_A + I_G\right) + \alpha_1 I_A + I_{CO1} + I_{CO2}$$

$$\therefore I_A - \alpha_2 I_A - \alpha_1 I_A = \alpha_2 I_G + I_{CO1} + I_{CO2}$$

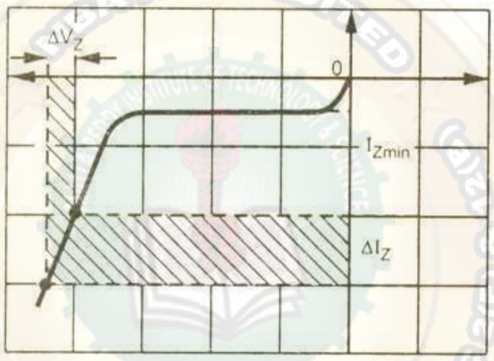
$$\therefore I_A = \frac{\alpha_2 I_G + I_{CO1} + I_{CO2}}{1-\left(\alpha_1 + \alpha_2\right)}$$

In blocking state α_1 and α_2 are small. Thus I_A is small.

As $\alpha_1 + \alpha_2$ approaches unit, the SCR is ready to enter into conduction. Thus due to positive gate current, the regenerative action takes place and SCR conducts.

Varactor Diode:

- We know that the transition capacitance c(t) is given by c(t)= $\frac{\varepsilon A}{\omega}$
- In both alloy junction diode and grown junction diode as the magnitude of the reverse bias increases, the width 'w' of the transition region increases, and the junction capacitance c(t) reduces.
- The voltage- variable nature of transition capacitance of reverse-biased pn- junction may be utilized in several applications such as
  1) In voltage tuning of an LC resonant.
  2) Self balancing bridge circuits.
  3) In parametric amplifiers etc.
  4) FM radio and TV receivers, AFC circuits.
  5) Used in adjustable band pass filters.
- This special diode is made especially for the above applications which are biased on the voltage- variable capacitance are called "Varactor diode" or "Varicap" or "Voltacap".



- Varactor diode symbol and circuit models are shown below.

Rs: Body series resistance.

C(t): Barrier capacitance.

R_r : Reverse diode resistance.

- Typically, at a reverse bias of 4v,

  C(t)= 20pF, R(s)=8.5 ohms, R(r)>1M (usually neglected).

Tunnel diode:

- A normal pn-junction has an impurity concentration of about 1 part in 10^8. With this amount of doping, the width of depletion layer, which constitutes the potential barrier of the junction, is of the order of 5 microns ($5x10^{-4}$ cm).
- If the concentration of impurity atoms is greatly increased, say 1 part in 10^3 the device characteristics are completely changed. The new diode was announced in 1958 by Leo Esaki. This diode is called 'Tunnel diode' or 'Esaki diode'.
- The barrier potential VB is related with the width of the depletion region with the following equation.

$$V_B = \frac{q\,N_A}{2\in}.\omega^2 \qquad \Rightarrow \omega^2 = \frac{2V_B \in}{q\,N_A}.$$

- From the above equation the width of the barrier varies inversely as the square root of impurity concentration.
- As the depletion width decreases there is a large probability that an electron will penetrate through the barrier. This quantum mechanical behavior is referred to as tunneling and hence these high impurity density pn-junction devices are called Tunnel diodes. This phenomenon is called as 'tunneling'.

Energy band structure of heavily doped pn-junction diode under open circuited conditions:

In the energy band structure for the lightly doped pn-diode, the Fermi level E_f lies inside the forbidden energy gap. In the heavily doped pn-diode E_f lies out side the forbidden band.

We know that, Ef = Ec – KT ln(Nc/ND)

For a lightly doped semiconductor, N_D<Nc, So that $\ln\left(\frac{N_c}{N_D}\right)$ is a positive number. Hence E_f < Ec, and the Fermi level lies inside the forbidden band.

For a heavily doped semiconductor donor concentrations are more so that, N_D> Nc and is $\ln\left(\frac{N_c}{N_D}\right)$ a negative number. Hence E_f > Ec, and the Fermi level lies outside the forbidden band.

Similarly, $E_f = E_V + KT\ln\left(\frac{N_V}{N_A}\right).$

For heavily doped p-region, N_A> N_V, and the Fermi-level lies in the Fermi-level lies in the valance band.

The energy band structure in a heavily doped pn-diode under open circuited condition is shown in the figure.

We have $$E_G = KT\ln\left(\frac{N_C N_V}{n_i^2}\right)$$

$$E_O = KT\ln\left(\frac{N_D N_A}{n_i^2}\right)$$

Comparing above two equations for heavily doped pn-diode we find that E_O>E_G. Therefore, the contact difference of potential energy E_O exceeds the forbidden energy gap voltage E_G.

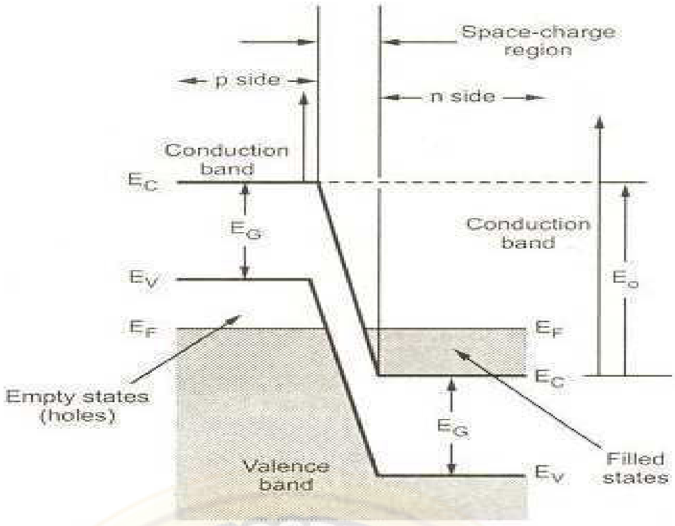


Fig. energy band in a heavily doped pn-diode under open circuited condition.

The Fermi level E_f in the p-side is at the same energy as the Fermi level Ef in the n-side. Note that there are no filled states on one side of the junction which are at the same energy as empty allowed states on the other side. Hence there can be no flow of charge in either direction across the junction, and the current is zero for an open circuited diode.

The volt-ampere characteristic:

If a reverse bias voltage is applied to the tunnel diode, the height of the barrier is increased above the open-circuit value EO. Hence the n-side levels must shift downward with respect to the p-side levels as shown in the figure below.

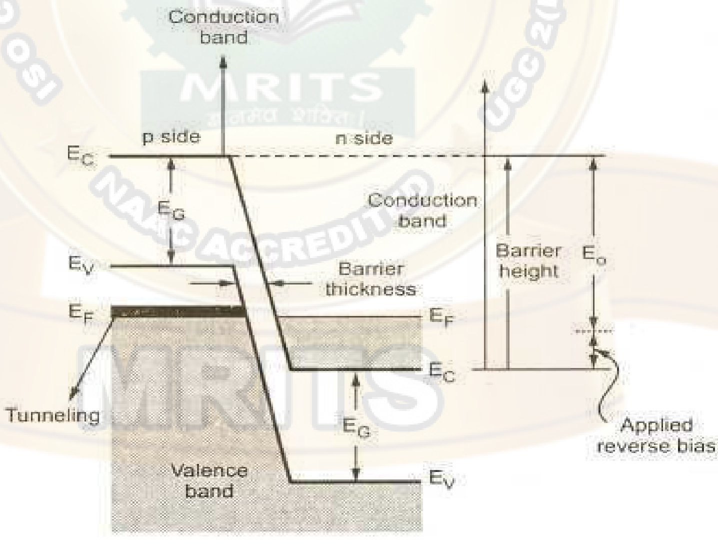


Fig. Under applied reverse bias

We now observe that there are some energy states in the valance band of the p-side which lie at the same level as allowed empty states in the conduction band of the n-side. Hence these electrons will tunnel from the p to the n-side, giving rise to a reverse diode current. As the magnitude of the reverse bias increase, causing the reverse current to increase.

Consider if a forward bias is applied to the diode so that the potential barrier is decreased below Eo. Hence the n-side levels must shift upward with respect to those on the p-side.

The energy band diagrams for a heavily doped under forward bias conditions are shown in figure below.

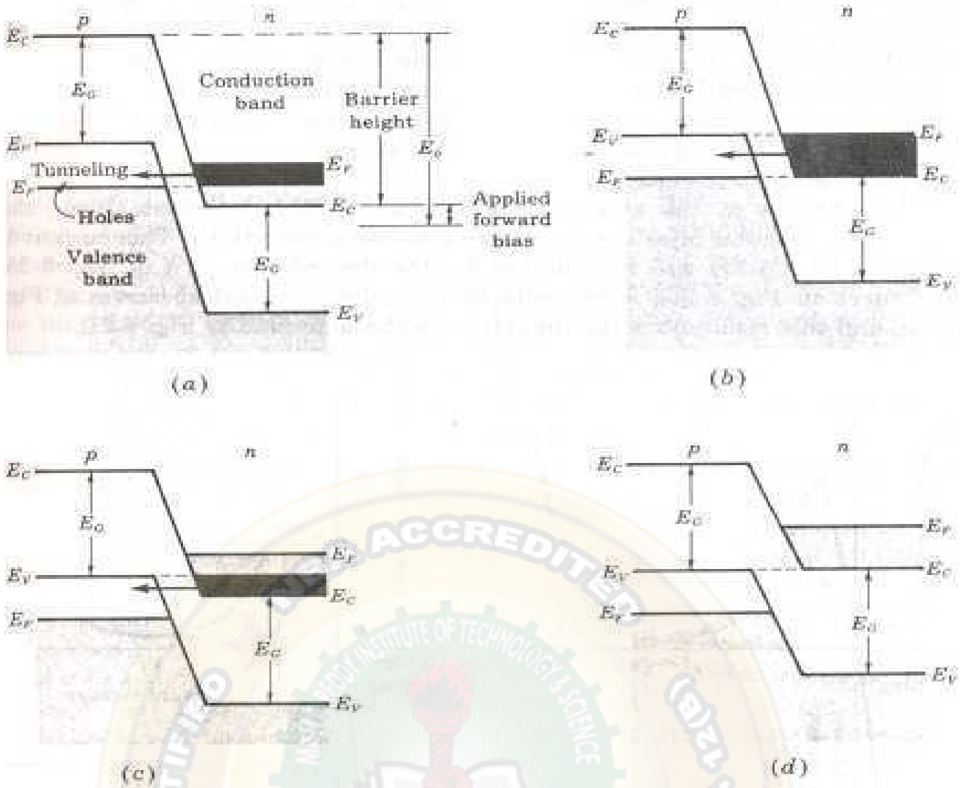


Fig. As the bias is increased, the band structure changes progressively from (a) to (d).

From fig (a) we can observe that the electrons will tunnel from the n to the p material giving rise to the forward current. As the forward bias is increased further, the maximum number of electrons can leave from occupied states on the right side of the junction, and tunnel through the barrier to the empty states on the left side of the junction giving rise to the peak current Ip.

If still more forward bias is applied, fig© is obtained and the tunneling current decreases. Finally if the forward bias is larger there is no9 empty allowed states on one side of the junction at the same energy as occupied states on the other side, the tunneling current must drop to zero.

The v-I characteristics of tunnel diode is shown in fig.

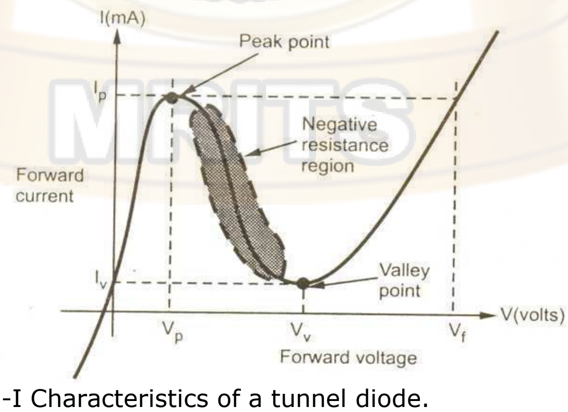


Fig.-I Characteristics of a tunnel diode.

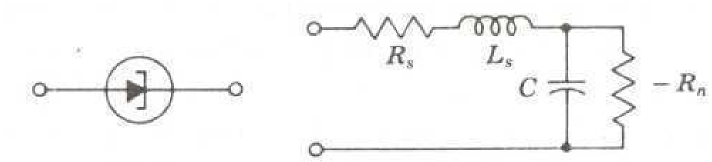
The tunnel diode exhibits a negative resistance characteristics between peak current Ip and valley current Iv. The tunnel diode is excellent conductor in the reverse bias conditions.

By applying small forward bias voltage to the tunnel diode the current increases and reaches to the maximum level. The maximum for small forward bias voltage is called as 'peak current (Ip)'.The corresponding voltage to the peak current is called 'peak voltage (Vp)'.

If forward bias voltage is increased beyond the peak voltage the current starts decreasing and reaches to the maximum level. This minimum value of the current is called as "valley current (Iv)". The corresponding voltage to the valley current is called as "valley voltage (Vv)".

If forward bias voltage is increased beyond valley voltage it exhibits the same characteristics as ordinary diode.

The tunnel diode symbol and small-signal model are shown in fig. below.

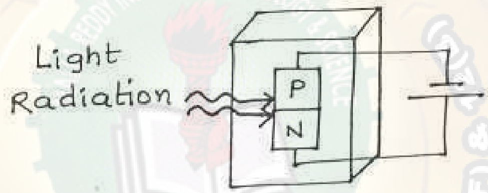


Applications of Tunnel diode:

1. It is used as a very high speed switch, since tunneling takes place at the speed of light.
2. It is used as a high frequency oscillator.

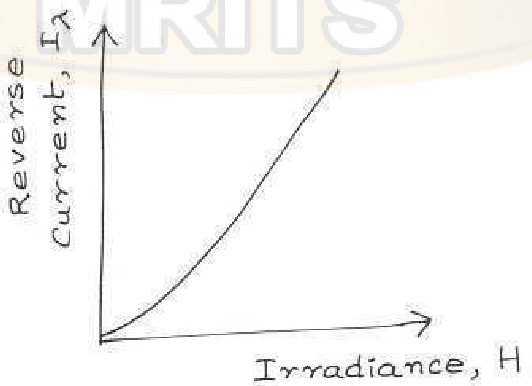
Photodiode:

The photodiode is a device that operates in reverse diode. The photodiode has a small transparent window that allows light to strike one surface of the pn-junction, keeping the remaining sides unilluminated.



The symbol of photodiode is shown in figure below.

A photodiode differs from a rectifier diode in that when its pn-junction is exposed to light, the reverse current increases with the light intensity. When there is no incident light the reverse current, I_λ, is almost negligible and is called the dark current. An increase in the amount of light intensity, expressed as irradiance (mW/cm^2), produces an increase in the reverse current.



Typically, the reverse current is approximately 1.4 μA at a Reverse bias voltage of 10V with an irradiance of 0.5 mWcm².

Therefore $R_R = V_R / I_\lambda$ = 10v/1.4μa = 7.14MΩ

At 20 mW/cm², the current is approximately 55 μa at VR=10v.

Therefore, $R_R = V_R / I_\lambda$ = 10v/55 μa = 182KΩ

Hence the photodiode can be used as a variable-resistance device controlled by light intensity.

The volt-ampere characteristics of photodiode are shown in figure.

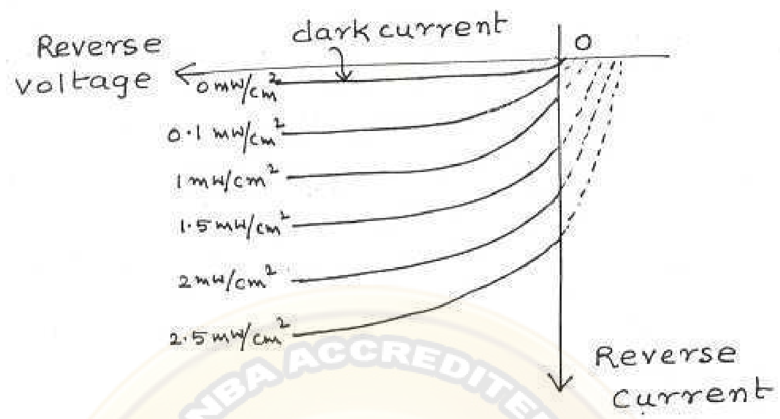


Fig. V-I characteristics of photo diode.

Advantages of Photo diodes:

1. It can be used as variable-resistance device.
2. Highly sensitive to the light.
3. The speed of operation is very high.

Disadvantages of Photo diodes:

1. The dark current is temperature dependent.

Applications of photodiode:

1) Photodiodes are commonly used in alarm systems and counting systems.
2) Used in demodulators.
3) Used in encoders.
4) Used in light detectors.
5) Used in optical communication systems.

UNIT - II

K. Kavya
Jyothsna

Combinational Logic circuits

1/ **Basic Theorems & properties of Boolean Algebra :-**

Duality :- Dual of relation $A+\bar{A}=1$ & $A\cdot\bar{A}=0$.
Duality is a very important property of Boolean algebra.

Basic Theorems :-

Theorem ① $A+A=A$ $\quad 0+0=0,\ 1+1=1 \Rightarrow A+A=A$

Proof :- $A+A=(A+A)\cdot 1$
$=(A+A)\cdot(A+\bar{A}) = AA + A\bar{A} + AA + A\bar{A} = A(1+1) = A$

Theorem ② :- $A\cdot A = A$ $\quad 0\cdot 0=0,\ 1\cdot 1=1$

Proof :- $A\cdot A = A\cdot A + 0$
$= AA + A\bar{A}$
$= A(A+\bar{A}) = A\cdot 1 = A$

Theorem ③ :- $A+1=1$ $\quad 1+0=1,\ 1+1=1 \Rightarrow 1+A=1$ or $A+1=1$

$\because A+(B\cdot C)=(A+B)\cdot(A+C)$

Proof :- $A+1 = 1\cdot(A+1)$
$=(A+\bar{A})(A+1) = A+\bar{A}\cdot 1$
$= A\cdot A + A + \bar{A}A + \bar{A} = A+\bar{A} = 1$

Theorem ④ :- $A\cdot 0 = 0$.

Theorem ⑤ :- $\bar{\bar{A}} = A$

Theorem ⑥ :- $A+AB=A$

Proof :- $A+AB = A(1+B)$
$= A\cdot 1 = A$

Theorem ⑦ :- $A(A+B)=A$

Proof :- $A(A+B) = A\cdot A + A\cdot B$
$= A + AB = A$

Proof:- $A+\bar{A}B = A+AB+\bar{A}B$ by Theorem ⑥

$= A+B(A+\bar{A})$

$= A+B\cdot 1 = A+B.$

Theorem ⑨:- $A\cdot(\bar{A}+B) = AB.$

proof:- $A\cdot(\bar{A}+B) = (A+A\cdot B)\cdot(\bar{A}+B)$ by Theorem ⑥

$= A\bar{A} + AB + A\bar{A}B + ABB$

$= AB + ABB = AB + AB = AB$

Fundamental Postulates of Boolean Algebra:-

→ $0+0=0$ $0+1=1+0=1$

$1\cdot 1=1$ $1\cdot 0=0\cdot 1=0$

→ $(A+B)=(B+A)$
$(A\cdot B)=(B\cdot A)$ } commutative law

→ $A\cdot(B+C)=(A\cdot B)+(A\cdot C)$
$A+(B\cdot C)=(A+B)\cdot(A+C)$ } Distributed law

→ $A+\bar{A}=1$ Since $0+\bar{0}=0+1=1$
& $1+\bar{1}=1+0=1$

$A\cdot\bar{A}=0$ Since $0\cdot\bar{0}=0\cdot 1=0$
& $1\cdot\bar{1}=1\cdot 0=0$

Laws of Boolean Algebra:

Three of the basic laws of Boolean Algebra. The commutative laws, associative laws & the distributive laws.

Commutative Laws:-

Law ①:- $A+B = B+A$:- This states that the order in which the variables are ORed makes no difference. Therefore, the o/p. The truth tables are identical.. A OR B is same as B OR A

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

B	A	B+A
0	0	0
0	1	1
1	0	1
1	1	1

2

Law ②:- $AB = BA$:- The commutative law of multiplication states ~~that the order~~ in which the variables are ANDed makes no difference in the o/p. The truth tables are identical. Therefore, A AND B is same as B AND A.

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

B	A	B.A
0	0	0
0	1	0
1	0	0
1	1	1

Associative law:

Law ① $A+(B+C)=(A+B)+C$: This law states that oring of several variables, the result is the same regardless of the grouping of the variables. For three variables, A OR B ORed with C is the same as A ORed with B OR C.

A B C	A+B	(A+B)+C
0 0 0	0	0
0 0 1	0	1
0 1 0	1	1
0 1 1	1	1
1 0 0	1	1
1 0 1	1	1
1 1 0	1	1
1 1 1	1	1

A B C	B+C	A+(B+C)
0 0 0	0	0
0 0 1	1	[illegible]
0 1 0	1	[illegible]
0 1 1	1	1
1 0 0	0	[illegible]
1 0 1	1	1
1 1 0	1	1
1 1 1	1	[illegible]

Law ②: $(AB)C=A(BC)$: The associative law of multiplication states that it makes no difference in order the variables are grouped when ANDing several variables. For three variables, A AND B ANDed with C is the same as A ANDed with B AND C.

A B C	AB	(AB)C
0 0 0	0	0
0 0 1	0	0
0 1 0	0	0
0 1 1	0	0
1 0 0	0	0
1 0 1	0	0
1 1 0	1	0

A B C	BC	A(BC)
0 0 0	0	0
0 0 1	0	0
0 1 0	0	0
0 1 1	1	0
1 0 0	0	0
1 0 1	0	0
1 1 0	0	0
1 1 1	1	1

Distributive law:

law : $A(B+C) = AB + AC$: The distributive law states that ORing several variables and ANDing the result with a single variable is equivalent to ANDing the result with a single variable with each of the several variables & then ORing the products

A	B	C	(B+C)	A·(B+C)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

A B C	A·B	A·C	AB+AC
000	0	0	0
001	0	0	0
010	0	0	0
011	0	0	0
100	0	0	0
101	0	1	1
110	1	0	1
111	1	1	1

Demorgan's theorems:

Demorgan suggested two theorems that form an important part of Boolean algebra.

They are

1) $\overline{AB} = \overline{A} + \overline{B}$: The complement of a product is equal to the sum of the complements

A	B	$\overline{AB}$	$\overline{A}+\overline{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

2) $\overline{A+B} = \bar{A}\,\bar{B}$:- The complement of a sum is equal to the product of the complements

A	B	$\overline{A+B}$	$\bar{A}\cdot\bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

Canonical & standard forms :-

Boolean expressions are constructed by connecting Boolean constants & variables with the Boolean operations. These Boolean expressions are also known as Boolean function. Boolean function is written as $f(A,B,C)$ or f

Ex:- Boolean function

$f(A,B,C) = (\overline{A+B})C$ or $f = (\overline{A+B})C$

Let us consider the four variable Boolean function

$$f(A,B,C,D) = A + \bar{B}\cdot C + A\cdot\bar{C}\bar{D}$$

(product terms: $\bar{B}\cdot C$, $A\cdot\bar{C}\bar{D}$; literals: A, $\bar{B}$, C, A, $\bar{C}$, $\bar{D}$)

Each occurrence of a variable in either a complemented or an uncomplemented form is called a Literal.

A product term is defined as either a literal or a product of literals.

$f(A,B,C,D) = (B+\bar{D}) \cdot (A+\bar{B}+C) \cdot (\bar{A}+C)$ (4)

Literals

A sum term is defined as either a literal or a sum of literals.

Literals & terms are in two forms:-

→ sum of product form (SOP) &

→ product of sum form. POS

Sum of product form:- The words sum & product are derived from the symbolic representation of the OR & AND functions by + & ·. A product term is any group of literals that are ANDed together.

For example:- ABC, xy & so on

A sum term is any group of literals that are ORed together. ex:- A+B+C, x+y & so on

A sum of product (SOP) is a group of product terms ORed together.

ex:- 1) $f(A,B,C) = ABC + A\bar{B}\bar{C}$ (sum; product terms)

2) $f(P,Q,R,S) = \bar{P}Q + QR + RS$ (sum; product terms)

Product of sum form :- (POS)

A product of sums is any group of sum terms ANDed together.

Ex:- 1) $f(A,B,C) = (A+B) \cdot (\bar{B}+C)$

(Product; Sum terms)

2) $f(P,Q,R,S) = (P+Q) \cdot (R+\bar{S}) \cdot (P+S)$

(Product; Sum terms.)

Canonical form (Standard SOP & POS forms) :-

The canonical forms are the special case of SOP & POS forms. These are also known as standard SOP & POS forms.

Standard SOP form or minterm canonical form :-

If each term in SOP form contains all the literals then the SOP form is known as standard or canonical SOP form. Each individual term in the standard SOP form is called minterm. Therefore, canonical SOP form is also known as minterm canonical form.

ex:- $f(A,B,C) = \bar{A}BC + A\bar{B}C + AB\bar{C}$

Each product term consists of all literals in either complemented form or uncomplemented form.

Standard POS form or maxterm canonical form :-

If each term in POS form contains all the literals the POS form is known as standard or

Standard canonical POS form.

nical POS form. Each individual term in the standard POS form is called Maxterm. Therefore canonical POS form is also known as maxterm canonical form.

M.

Ex:- $f(A,B,C) = (A+B+C) \cdot (A+\bar{B}+C)$

Each sum term consists of all literals in either complemented form or uncomplemented form.

$f(A,B,C) = \Sigma m$ - SOP -

$f(A,B,C) = \Pi M$ - POS -

duct-of-Sums Simplification:-

Examples

① $ABCD + ABD = ABD(C+1)$ $(\because A+1 = A)$ $(A \cdot 1 = A)$

$= ABD \cdot 1 = ABD$

② $ABCD + A\bar{B}CD = ACD(B+\bar{B})$ $(\because B+\bar{B}=1)$ $A \cdot 1 = A$

$= ACD \cdot 1$

$= ACD$

③ $XY + XYZ + XY\bar{Z} + \bar{X}YZ$

$= XY(1+Z) + XY\bar{Z} + \bar{X}YZ$ $A+1=1$

$= XY + XY\bar{Z} + \bar{X}YZ$

$= XY(1+\bar{Z}) + \bar{X}YZ$

$= XY + \bar{X}YZ$

$= Y(X+\bar{X}Z)$ $\because A+\bar{A}B = A+B$

$= Y(X+Z)$

④ $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC$

$= \bar{A}\bar{C}(\bar{B}+B) + \bar{A}BC$ $(A+\bar{A}=1)$

$= \bar{A}\bar{C} + \bar{A}BC$

$= \bar{A}(\bar{C}+BC) = \bar{A}(\bar{C}+B)$

⑤ $ABC + A\bar{B}C + AB\bar{C} = A(C+B)$

LHS $= ABC + A\bar{B}C + AB\bar{C}$

$= AC(B+\bar{B}) + AB\bar{C}$ $\because A+\bar{A}B = A+B$

$= AC + AB\bar{C}$

$= A(C+B\bar{C}) = A(C+B)$

$=$ R.H.S

⑥ $\bar{A}BC\bar{D} + BC\bar{D} + B\bar{C}\bar{D} + B\bar{C}D$

$= BC\bar{D}(\bar{A}+1) + B\bar{C}\bar{D} + B\bar{C}D$

$= BC\bar{D} + B\bar{C}\bar{D} + B\bar{C}D$

$= B\bar{D}(C+\bar{C}) + B\bar{C}D$

$= B\bar{D} + B\bar{C}D$

$= B(\bar{D}+\bar{C}D)$ $(\because A+\bar{A}B = A+B)$

$= B(\bar{D}+\bar{C})$

⑦ $AC + C(A+\bar{A}B) = AC + AC + \bar{A}BC$ $(A+A=A)$

$= AC + \bar{A}BC$

$= C(A+\bar{A}B)$ $A+\bar{A}B = A+B$

$= C(A+B)$

⑧ $\bar{A}B\bar{C}D + \bar{A}BCD + ABD = \bar{A}BD(\bar{C}+C) + ABD$

$= \bar{A}BD + ABD$

$= BD(\bar{A}+A)$ $(A+\bar{A}=1)$

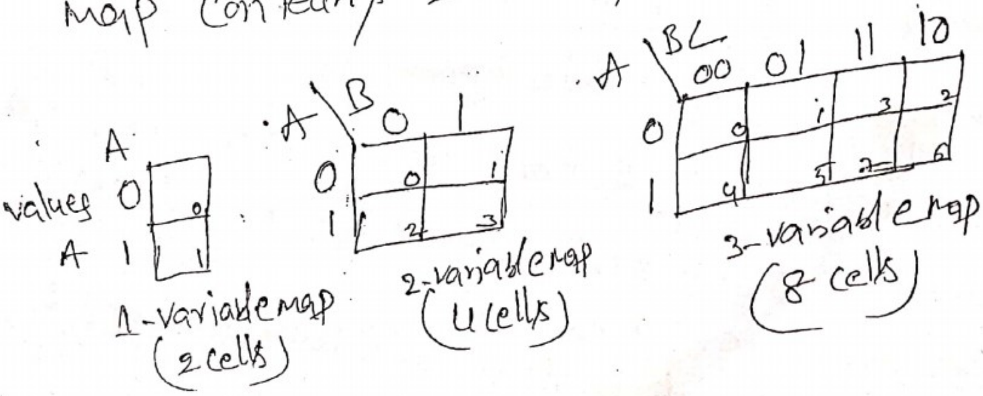
$= BD$

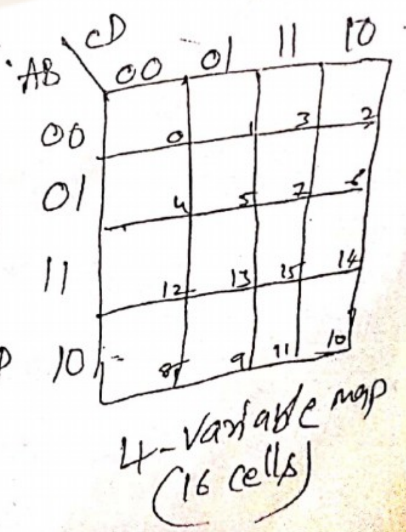
Map ... The B... boolean ... functi... re...

Map method :-

The Boolean functions can be simplified by
lean laws, rules & Theorems, the simplification of Boolean
ction is very important as it saves the Hardware
uired & hence the cost for design of specific Boolean
nction. on the other hand, the map method gives
s a systematic approach for simplifying a Boolean
expression. The map method, first proposed by Veitch
& Modified by Karnaugh, hence it is known as the
Veitch diagram or the Karnaugh map.

ne-variable, Two-variable, Three-variable & four variable
Maps :- The basis of this method is graphical chart
known as Karnaugh map (K-map). It contains boxes
called cells. Each of the cell represents one of the
2^n possible products that can be formed from n variables.
Thus, a 2-variable map contains $2^2 = 4$ cells, a 3-variable
map contains $2^3 = 8$ cells & so forth.

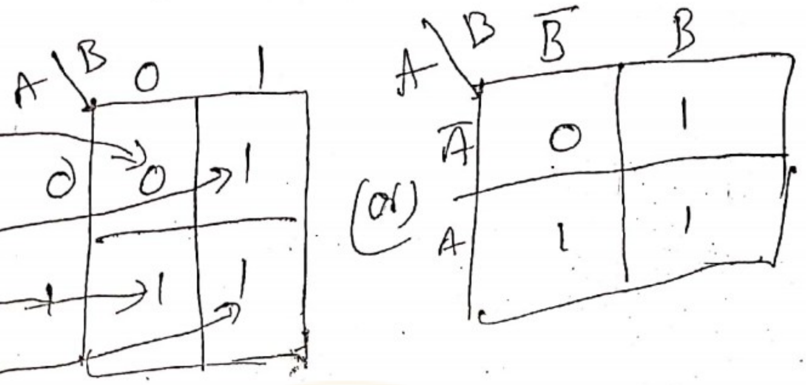




Representation of Truth table on Karnaugh Map (K-map)

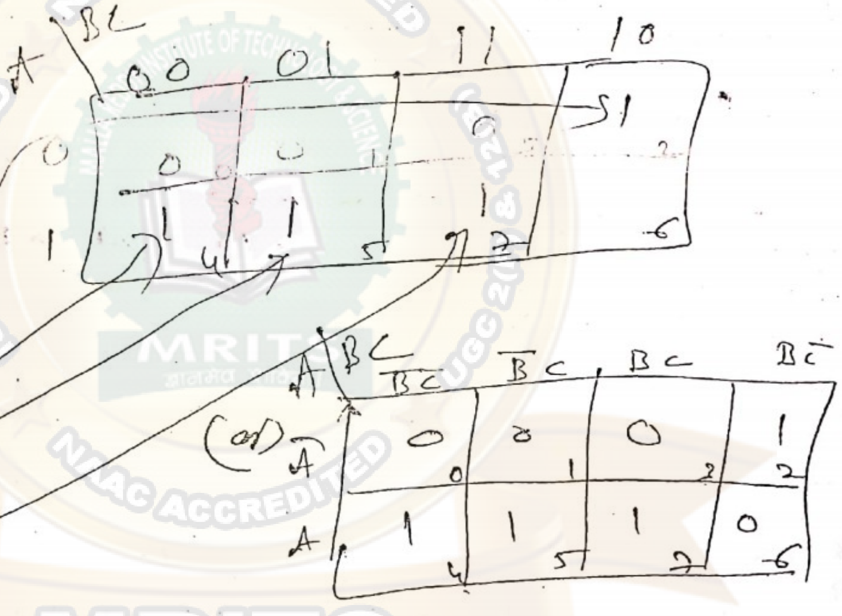
K-maps plotted from truth table 2 & 3-variables

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



2-variables

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1



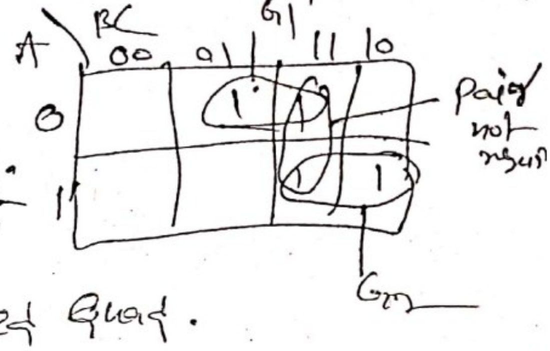
3-variables

Grouping cells for simplification:-

1) Grouping Two Adjacent ones (pair)
   - → pair of vertically & horizontally adjacent 1's.
   - → cell in the left most column & right most column are considered to be adjacent
   - → the top row & bottom row are considered to be adjacent

two overlapping pair of 1s considered. (7)

-> Three group of pairs can be formed, But only two pairs are enough to include all 1's present in the K-map



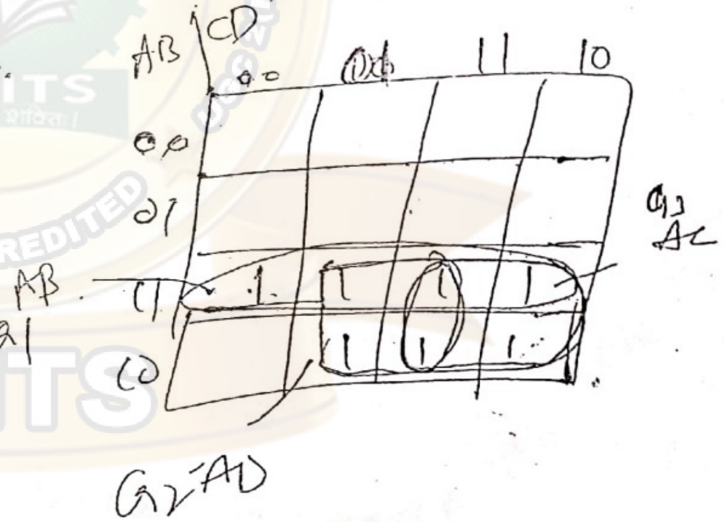
2) Grouping Four adjacent ones (Quad):-

-> Group of Four adjacent 1's called Quad.

-> Four 1s are horizontally adjacent & vertically adjacent

-> Four 1's are in a square & they are considered adjacent to each other.

-> Four 1's, top & bottom rows are considered & left most & right most columns are also adjacent to each other.



3) Grouping Eight Adjacent ones (octet):-

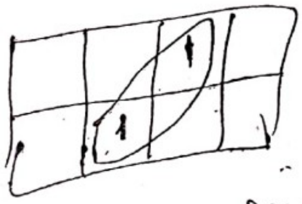
Group of eight adjacent 1's called octet.

-> 8 1's are horizontally & vertically adjacent

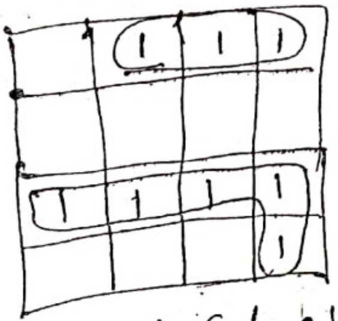
-> left most & right most cells are adjacent

-> top & bottom cells are adjacent.

Illegal Groupings:



Diagonal Grouping is illegal

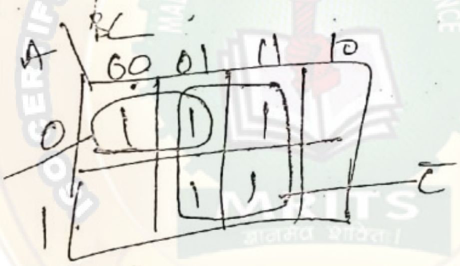


Grouping of odd number of cells is illegal.

→ Prime Implicants & K-maps:-

Ex: obtain the prime implicants for given Boolean expression using K-map $f(A,B,C) = \Sigma(0,1,3,5,7)$

Sol:



$G_1: \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C$

$\bar{A}\bar{B}(C+\bar{C}) = \bar{A}\bar{B}$

$G_2: \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + ABC$

$= \bar{A}C(B+\bar{B}) + AC(\bar{B}+B)$

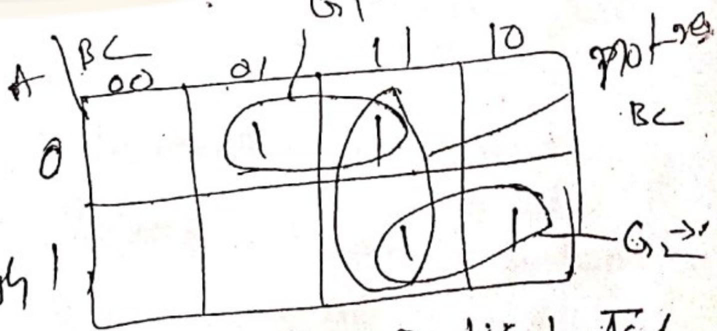
$= \bar{A}C + AC$

$= C(\bar{A}+A) = C$

$f(A,B,C) = \bar{A}\bar{B} + C$

The prime implicants for given Boolean expression are $\bar{A}\bar{B} + C$.

Essential prime Implicants:



The three prime implicants $\bar{A}C$, BC & AB. However, only two prime implicants: $\bar{A}C$ & AB are enough to include all 1's present in the K-map. Thus prime implicants $\bar{A}C$ & AB are called essential prime implicants. In general, we can say that the minimum number of prime implicants required to ie. all 1's present in the K-map are called

...ntial prime implicants.

Minimize the expression $Y = A\bar{B}C + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$.

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	1	1	1	
A 1	1	1		

Group1 $\Rightarrow \bar{A}C$

$= \bar{A}\bar{B}C + \bar{A}BC$

$= \bar{A}C(\bar{B}+B) = \bar{A}C$

G(1)

G(2) $= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$

$= \bar{A}\bar{B}(\bar{C}+C) + A\bar{B}(\bar{C}+C)$

$= \bar{A}\bar{B} + A\bar{B}$

$= \bar{B}(\bar{A}+A) = \bar{B}$

Group2 $= \bar{B}$

Minimize the expression

$Y = \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D + AB\bar{C}D + AB\bar{C}D + \bar{A}\bar{B}C\bar{D}$

Sol:

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00				1
$\bar{A}B$ 01	1	1		
AB 11	1	1		
$A\bar{B}$ 10		1		

G3 – $\bar{A}\bar{B}C\bar{D}$

G1 ⇒ $A\bar{C}D$

G2 ⇒ $B\bar{C}$

$Y = \bar{A}\bar{B}C\bar{D} + A\bar{C}D + B\bar{C}$

→ Reduce the following four variable function to its minimum sum of products form $Y = \bar{A}\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + A\bar{B}C\bar{D} + AB\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}$

Sol:-

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	1		1	1
$\bar{A}B$ 01				
AB 11	1			1
AB				

G-1 = $\bar{B}C$

G-2 = $A\bar{D}$

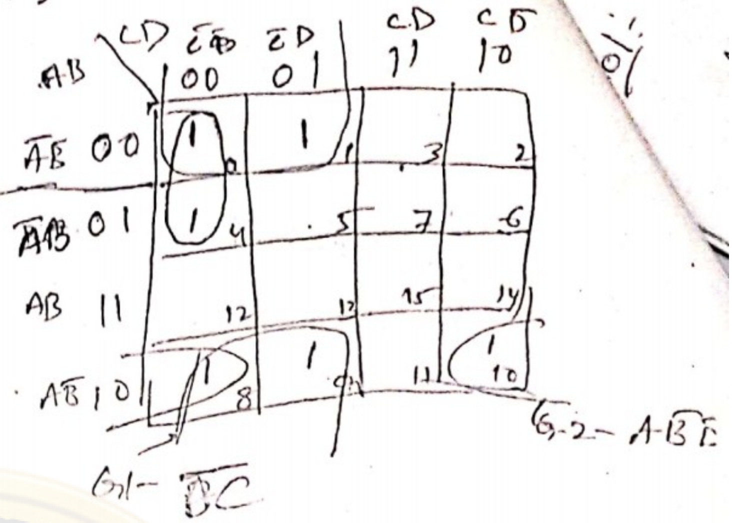
$Y = \bar{B}C + A\bar{D} + \bar{B}\bar{D}$

→ Reduce the following function using K-map Technique.

$f(A, B, C, D) = \Sigma m(0, 1, 4, 8, 9, 10)$.

Sol:

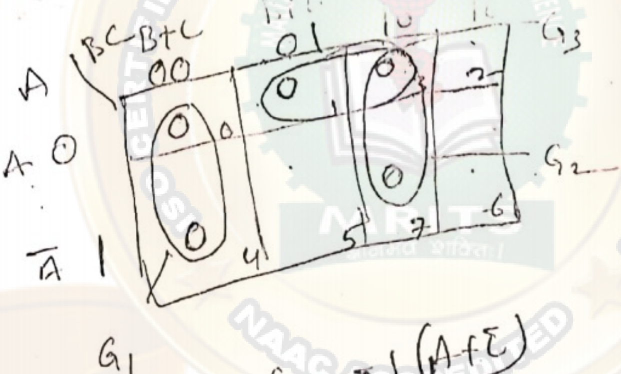
$f(A, B, C, D) = \bar{A}\bar{C}\bar{D} + A\bar{B}\bar{D} + \bar{B}\bar{C}$



→ minimize the expression

$Y = (A+B+C)(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+\bar{C})(\bar{A}+B+\bar{C})(A+B+C)$

Sol:



$G_1 = B+C$

$G_2 = \bar{B}+\bar{C}$

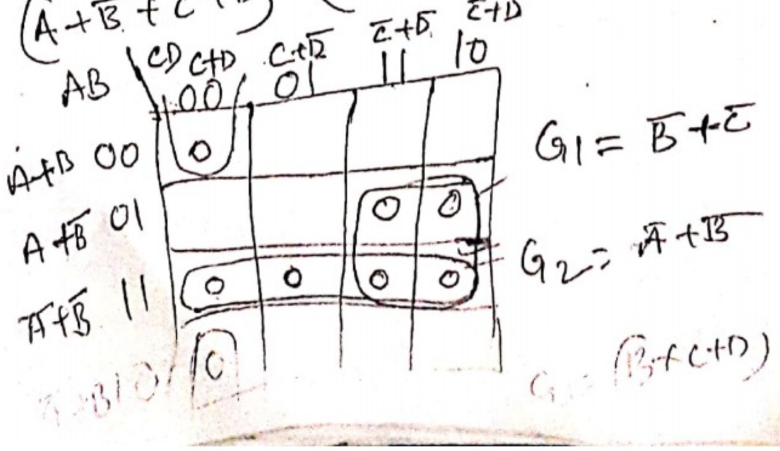
$G_3 = A+\bar{C}$

$Y = (B+C) \cdot (\bar{B}+\bar{C})(A+\bar{C})$

→ minimize the following expression in the POS form

$Y = (\bar{A}+\bar{B}+C+D)(\bar{A}+\bar{B}+\bar{C}+D)(\bar{A}+\bar{B}+\bar{C}+\bar{D})(\bar{A}+B+C+D)(A+\bar{B}+\bar{C}+\bar{D})(A+B+C+D)(\bar{A}+\bar{B}+C+\bar{D})(A+\bar{B}+\bar{C}+D)$

Sol:



$G_1 = \bar{B}+\bar{C}$

$G_2 = \bar{A}+\bar{B}$

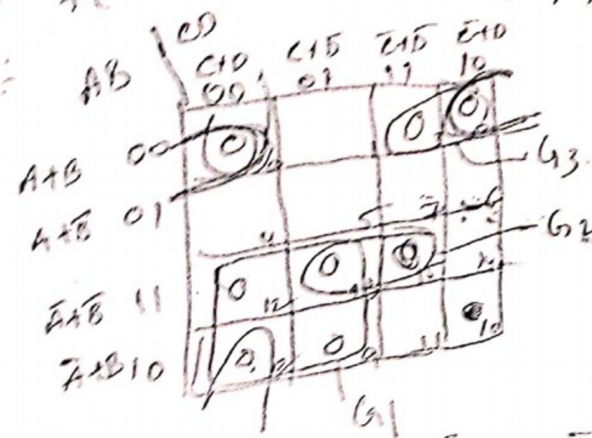
$G_3 = (B+C+D)$

$Y = (B+C+D) \cdot (\bar{B}+\bar{C}) \cdot (\bar{A}+\bar{B})$

...duce the following function using K-map technique. (9)

$f(A,B,C,D) = \prod M(0,2,3,8,9,12,13,15)$

Sol:



$G_1 = \bar{A}+C$

$G_2 = \bar{A}+\bar{B}+\bar{D}$

$G_3 = A+B+\bar{C}$

$G_4 = A+B+D$

$f = (\bar{A}+\bar{B}+\bar{D}).(A+B+\bar{C})(\bar{A}+C)(A+B+D)$

Don't Care Conditions:- In some logic circuits, certain input conditions never occur, therefore the corresponding output never appears. In such cases the o/p level is not defined, it can be either High & Low. These output levels are indicated by 'x' or 'd' in the truth tables & are called don't care outputs or don't care conditions or incompletely specified functions. These outputs are defined for input conditions from 000 to 101. For remaining two conditions of i/p, o/p is not defined, hence these are called don't care conditions for this truth table.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	x
1	1	1	x

A ckt designer is free to make the o/p for any "don't care" condition either a '0' or a '1' in order to produce the simplest o/p expression.

Describing Incomplete Boolean function:

In expression,

$$f(A,B,C) = \Sigma m(0,2,4) + d(1,5)$$

minterms are 0, 2 & 4. The additional term d(1,5) introduces to specify the don't care conditions. This term specifies that outputs for minterms 1 & 5 are not specified & hence these are don't care conditions. letter 'd' is used to indicate don't care conditions in the expression.

The above expression indicates how to represent don't care conditions in the minterm canonical formula.

In the similar manner, we can specify the don't care conditions in the maxterm canonical formula. For example

$$f(A,B,C) = \Pi M(2,3,7) + d(1,5)$$

Minimization of Incompletely specified Functions:

A circuit designer is free to make the output for any don't care condition either a '0' or '1' in order to produce the simplest output expression. Consider a truth table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	X
1	1	1	X

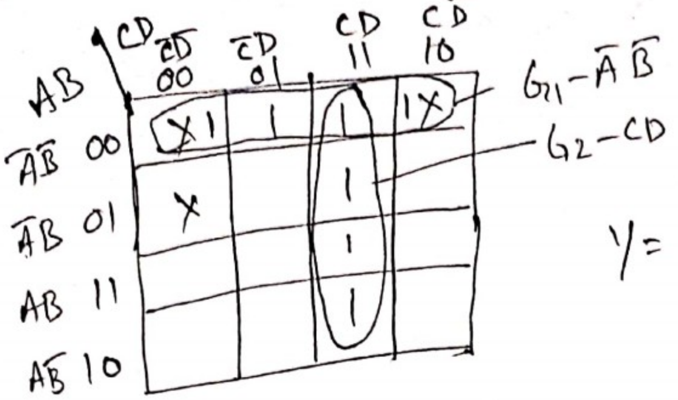
A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0		1	1	
A 1		1	X	X

$Y = C$

It is not always advisable to put don't cares as 1s. Here, the don't care o/p for cell ABC is taken as 1 to form a quad & don't care o/p for cell $AB\bar{C}$ is taken as 0, since it is not helping any in expression.

, the reduced SOP form of the following function

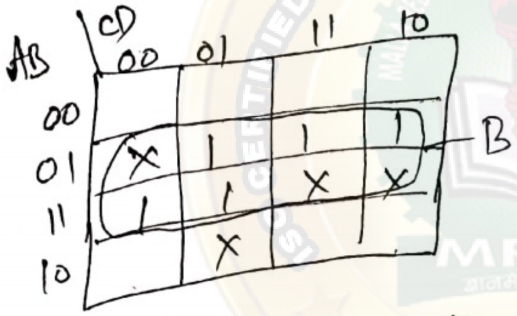
$(A, B, C, D) = \Sigma m(1, 3, 7, 11, 15) + \Sigma d(0, 2, 4)$



$Y = \bar{A}\bar{B} + CD.$

educe the following function using Karnaugh map technique

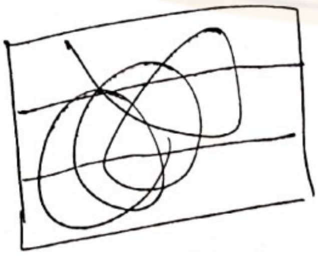
$f(A, B, C, D) = \Sigma m(5, 6, 7, 12, 13) + \Sigma d(4, 9, 14, 15)$

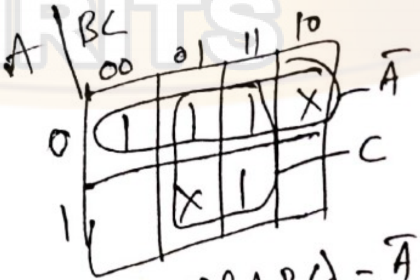


$f(A, B, C, D) = B.$

Reduce the following function using Karnaugh map technique $f(A, B, C) = \Sigma m(0, 1, 3, 7) + \Sigma d(2, 5)$

Sol:





$f(A, B, C) = \bar{A} + C.$

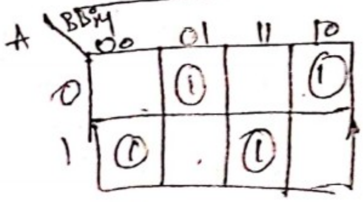
Full subtractor: A full-subtractor is a combinational circuit that performs a subtraction between two bits, taking into account borrow of the lower significant stage. This circuit has three inputs & two outputs. The three I/P, are A, B & B_{in}, denote the minuend, subtrahend, & previous borrow, respectively. The two outputs, D & B_{out}, represent the difference & O/P borrow, respectively.

0 − 0 = 0
0 − 1 = 1 B①
1 − 0 = 1
1 − 1 = 0

Inputs			O/Ps	
A	B	B_{in}	D	B_{out}
0	[illegible]	[illegible]	0	0
0	0	1	1	1
0	[illegible]	0	1	1
0	1	1	[illegible]	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	

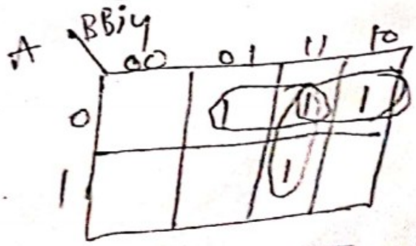
K-Map Simplification of D & B_{out}

For D



$D = \bar{A}\bar{B}B_{in} + \bar{A}B\bar{B}_{in} + ABB_{in}$

For B_{out}



$B_{out} = \bar{A}B_{in} + \bar{A}B + BB_{in}$

The Boolean function for D (Difference) can be further simplified as follows

$$D = \bar{A}\bar{B}B_{in} + \bar{A}B\bar{B}_{in} + A\bar{B}\bar{B}_{in} + ABB_{in}$$

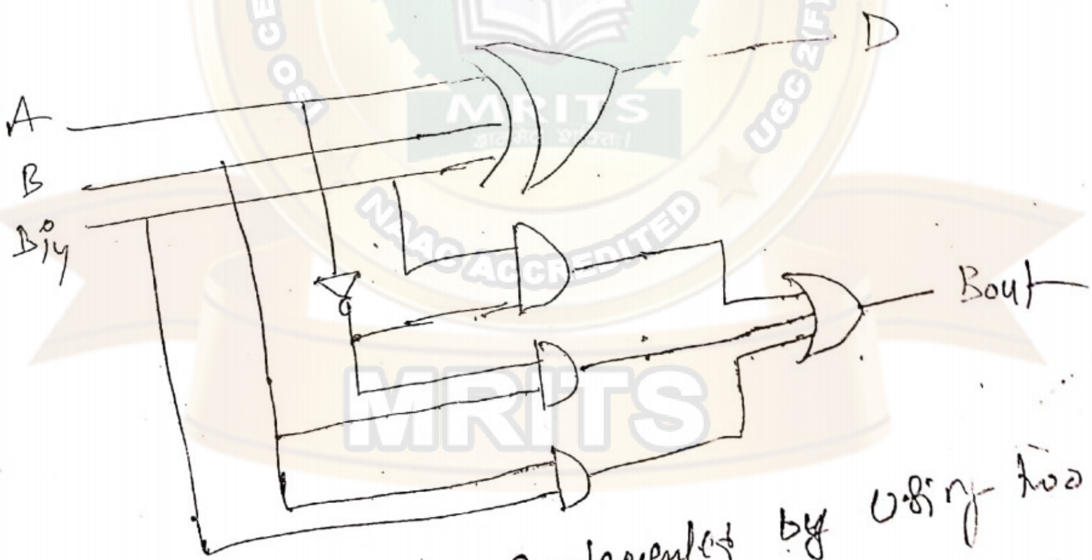
$$= B_{in}(\bar{A}\bar{B} + AB) + \bar{B}_{in}(\bar{A}B + A\bar{B})$$

$$= B_{in}(\overline{\bar{A}B + A\bar{B}}) + \bar{B}_{in}(A \oplus B)$$

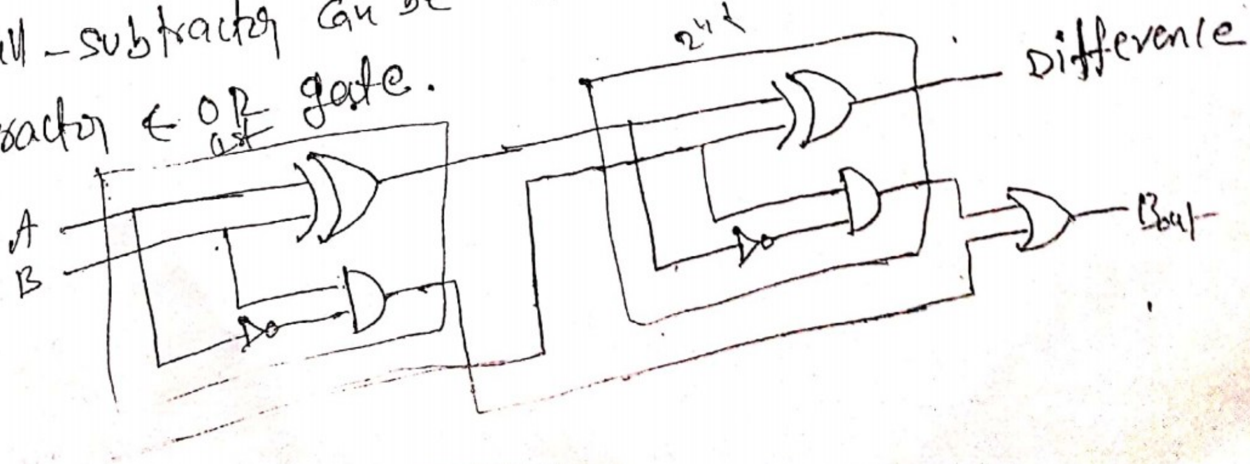
$$= B_{in}(\overline{A \oplus B}) + \bar{B}_{in}(A \oplus B)$$

$$= B_{in} \oplus (A \oplus B)$$

The simplified Boolean function circuit for full-subtractor can be implemented as shown in figure



A full-subtractor can be implemented by using two half-subtractors & OR gate.



Decimal (BCD) Adder

The digital systems handles the decimal number in the form of binary coded decimal number (BCD). A BCD adder is a circuit that adds two BCD digits & produces a sum digit also in BCD. BCD numbers use 10 digits 0 to 9 which are represented in the binary form 0000 to 1001, i.e. each BCD digit is represented as a 4-bit binary number. when we write BCD number say 526, it can be represented as

5	2	6
↓	↓	↓
0101	0010	0110

Here, we should note that BCD cannot be greater than 9.

The addition of two BCD numbers can be best understood by considering the three cases that occur when two BCD digits are added.

Sum equals 9 or less with carry 0:

Let us consider additions of 3 & 6 in BCD.

$$\begin{array}{r} 6 \\ +3 \\ \hline 9 \end{array} \qquad \begin{array}{r} 0110 \\ 0011 \\ \hline 1001 \end{array} \begin{array}{l} \leftarrow \text{BCD for 6} \\ \leftarrow \text{BCD for 3} \\ \leftarrow \text{BCD for 9} \end{array}$$

The addition is carried out as in normal binary addition & the sum is 1001, which is BCD code for 9.

Sum greater than 9 with carry 0:-

Let us consider addition of 6+8 in BCD

6	0110	← BCD for 6
+8	1000	← BCD for 8
14	1110	← invalid BCD number

The sum 1110 is an invalid BCD number. This has occurred because the sum of the two digits exceeds 9. Whenever this occurs the sum has to be corrected by the addition of six (0110) to the invalid BCD number as shown below

6	0110	← BCD for 6
+8	1000	← BCD for 8
14	1110	← invalid BCD number
	+ 0110	
	0001 0100	← BCD for 14
	1 4	

After addition of 6 carry is produced into the second decimal position.

Sum equals 9 or less with carry 1:-

Let us consider addition of 8+9 in BCD

8	1000	← BCD for 8
+9	1001	← BCD for 9
17	1 0001	← Incorrect BCD result

Boolean expression for the o/ps of half-subtractor are determined as follows.

K-map simplification for half-subtractor

For difference

A \ B	0	1
0		1
1	1	

For Borrow

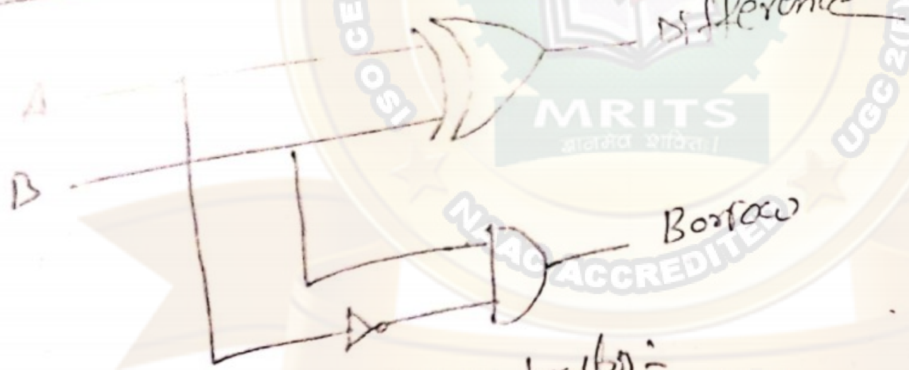
A \ B	0	1
0		1
1		

$Borrow = \bar{A}B$

$Difference = \bar{A}B + A\bar{B}$

$= A \oplus B$

Logic diagram



Limitations of Half-subtractor:-

In multidigit subtraction, we have to subtract two bits along with the borrow of the previous digit subtraction. Effectively such subtraction requires subtraction of three bits. This is not possible with half-subtractor.

Subtractors :-

The subtraction consists of Four possible elementary operations, namely,

0 - 0 = 0

0 - 1 = 1 with 1 borrow

1 - 0 = 1

1 - 1 = 0

In all operations, each subtrahend bit is subtracted from the minuend bit. In case of second operation the minuend bit is smaller than the subtrahend bit, hence 1 is borrowed. Just as there are half & full adders, there are half & Full-subtractors.

Half-subtractor:- A half-subtractor is a combinational circuit that subtracts two-bits & produces their difference. It also has an o/p to specify if a 1 has been borrowed. Let us designate minuend bit as A & the subtrahend bit as B. The result of operation A-B for all possible values of A & B is tabulated in below table

i/ps		o/ps	
A	B	Difference (D)	Borrow B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The half-subtractor has two i/p variables & two o/p variables

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Adder (4): Digital computers perform various arithmetic operations. The most basic operation, is the addition of two binary digits. This simple addition consists of four possible elementary operations, namely

$0+0=0$

$0+1=1$

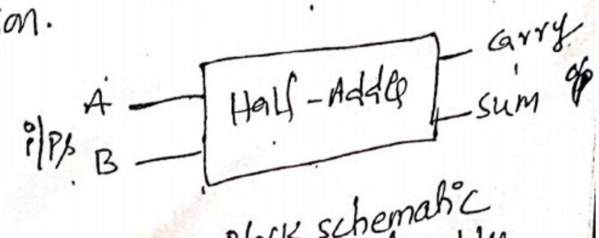
$1+0=1$

$1+1=10_2$

The first three operations produce a sum whose length is one digit but when the last operation is performed sum is two digits. The higher significant bit of this result is called a carry, & lower significant bit is called sum. The logic circuit which performs this operation is called a half-adder. The circuit which performs addition of three bits (two significant bits & a previous carry) is a full-adder.

Half-Adder: The half-adder operation needs two binary i/ps: augend & addend bits & two binary outputs: sum & carry. The truth table gives the relation between input & output variables for half-adder operation.

Inputs		Outputs	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
	0	0	



Block schematic of half-adder

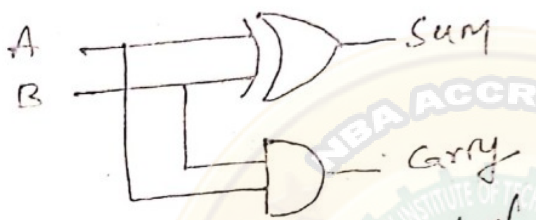
K-Map simplification for Carry + Sum

A \ B	0	1
0		
1		1

Carry = AB

A \ B	0	1
0		1
1	1	

$$sum = A\overline{B} + \overline{A}B$$
$$= A \oplus B.$$



logic diagram for half-adder

Limitations of Half-adder:- In multidigit addition we have to add two bits along with the carry of previous digit addition. Effectively such addition requires addition of three bits. This is not possible with half-Adder. Hence half-adders are not used in practice.

Full-Adder:- A Full-adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs + two outputs. Two of the input variables denoted by A + B, represent the two significant bits to be added, The third input Cin, represents the carry from the previous lower significant position. The truth table for full-adder is shown

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oolean function for sum can be further simplified as follows

$$Sum = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$

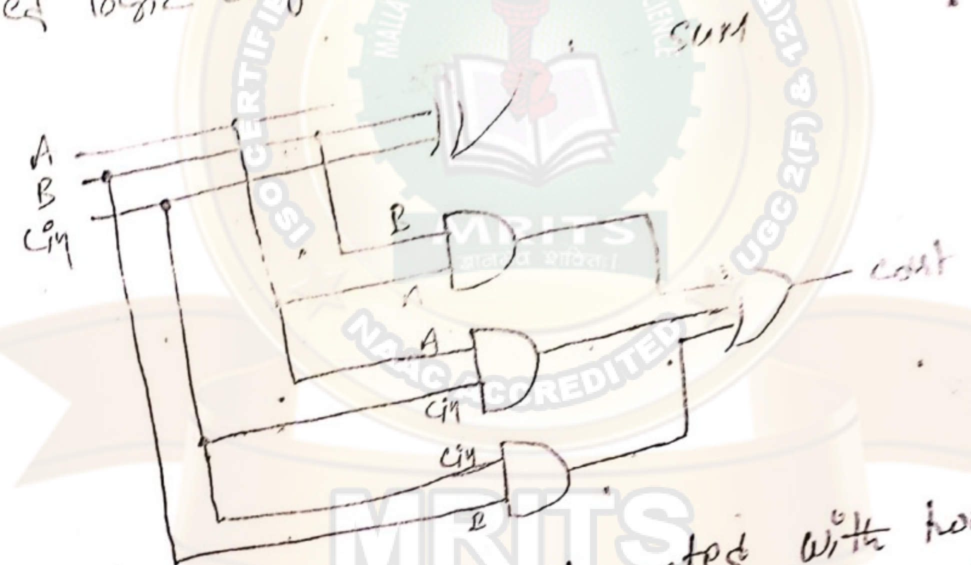
$$= C_{in}(\bar{A}\bar{B} + AB) + \bar{C}_{in}(\bar{A}B + A\bar{B})$$

$$= C_{in}(A \odot B) + \bar{C}_{in}(A \oplus B)$$

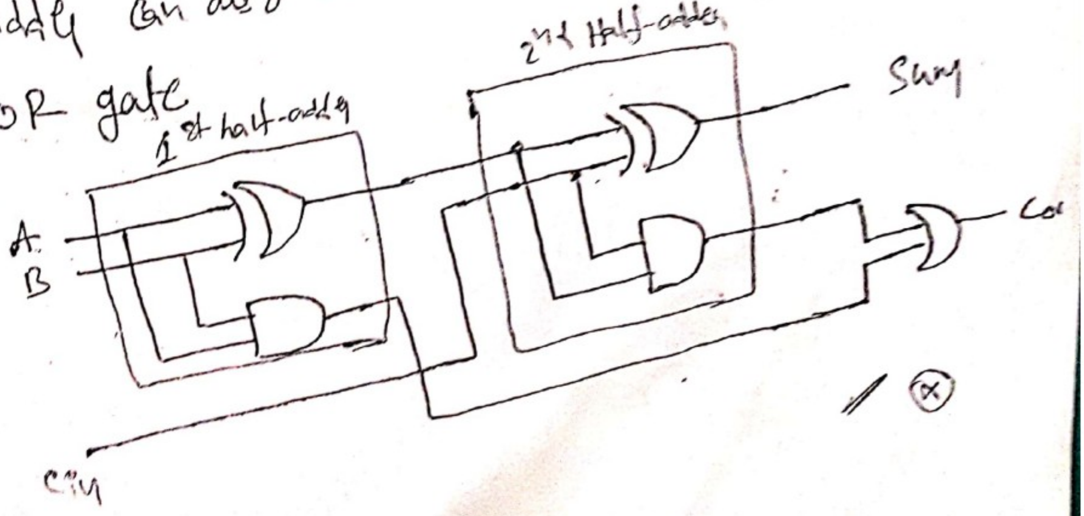
$$= C_{in}(\overline{A \oplus B}) + \bar{C}_{in}(A \oplus B)$$

$$= C_{in} \oplus (A \oplus B)$$

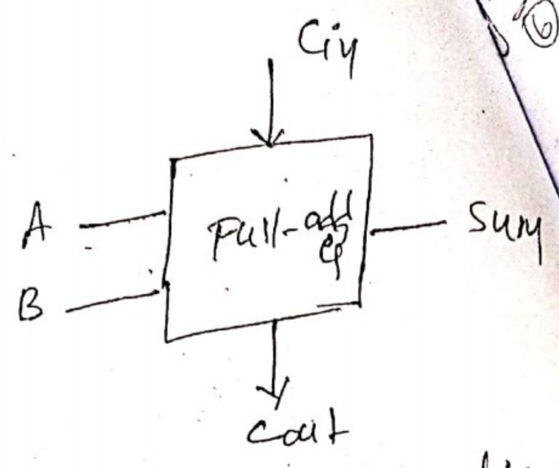
Simplified logic diagram for full-adder



A Full-adder can also be implemented with two half-adders & one OR gate



Inputs			Outputs	
A	B	C_{in}	Carry (C_{out})	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Block schematic of full-adder

K-Map simplification for Carry & Sum

For Carry (C_{out})

A \ BC_{in}	00	01	11	10
0			1	
1		1	1	1

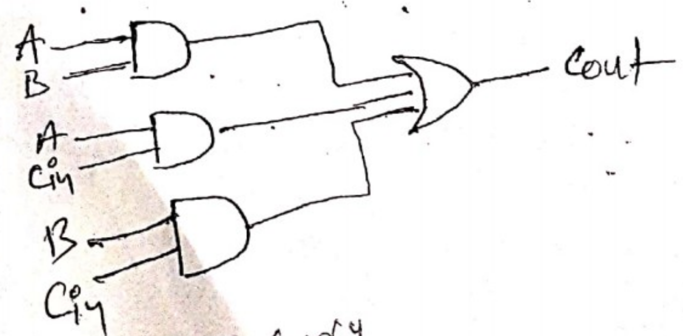
$C_{out} = AB + AC_{in} + BC_{in}$

For Sum

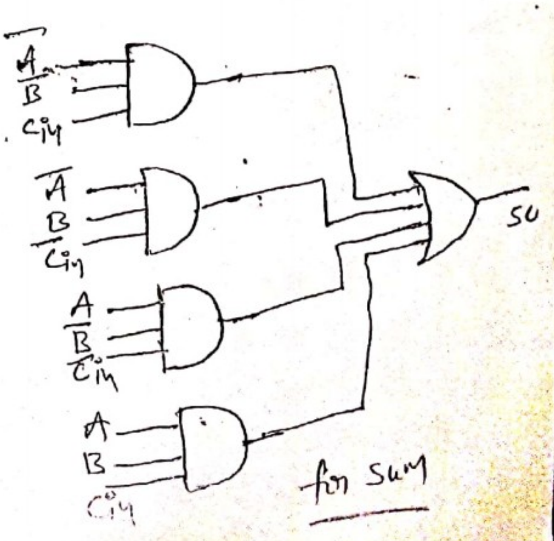
A \ BC_{in}	00	01	11	10
0		1		1
1	1		1	

$SUM = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$

Logic diagrams



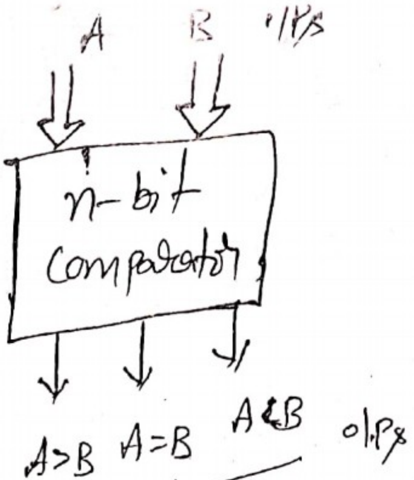
for Carry



for Sum

Magnitude comparator :-

(6) A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers. The block diagram of an n-bit comparator. It receives two n-bit numbers A & B as i/ps & o/ps are A > B, A = B & A < B. depending upon the relative magnitudes of the two number, one of the o/ps will be high



Block diagram of n-bit comparator

01 – 1
10 – 2
11 – 3

Design 2-bit comparator using gates:-

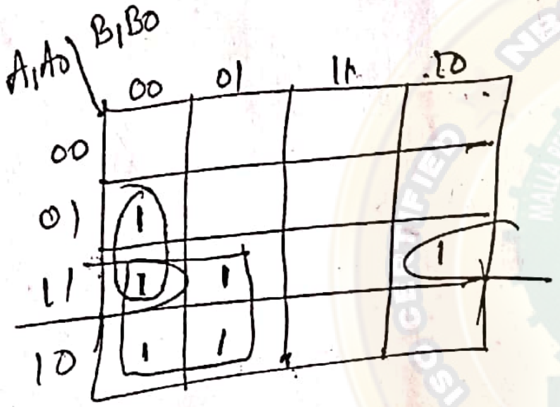
The truth table for 2-bit

i/ps				o/ps		
A		B				
A_1	A_0	B_1	B_0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	[illegible]	0	1	0

A_1	A_0	B_1	B_0	$A>B$	$A=B$	$A<B$
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

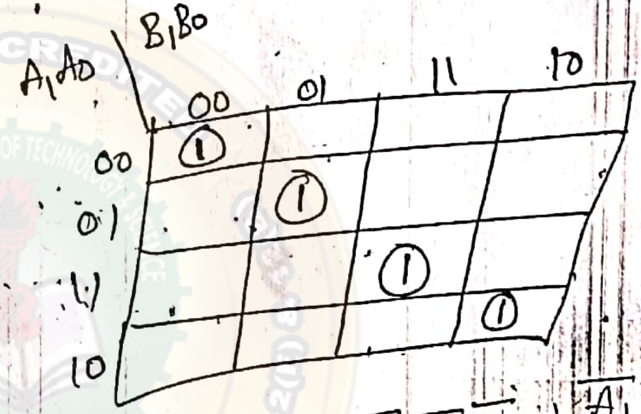
K-map simplifications

For $A>B$



$A>B = A_0\overline{B_1}\,\overline{B_0} + A_1\overline{B_1} + A_1 A_0 \overline{B_0}$

For $A=B$

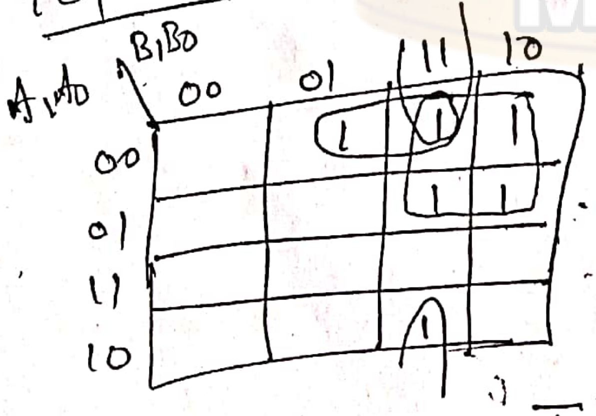


$(A=B) = \overline{A_1}\,\overline{A_0}\,\overline{B_1}\,\overline{B_0} + \overline{A_1} A_0 \overline{B_1}$
$+ A_1 A_0 B_1 B_0 + A_1 \overline{A_0} B$

$= \overline{A_1}\,\overline{B_1}(\overline{A_0}\,\overline{B_0} + A_0 B_0) +$
$A_1 B_1 (A_0 B_0 + \overline{A_0}\,\overline{B_0})$

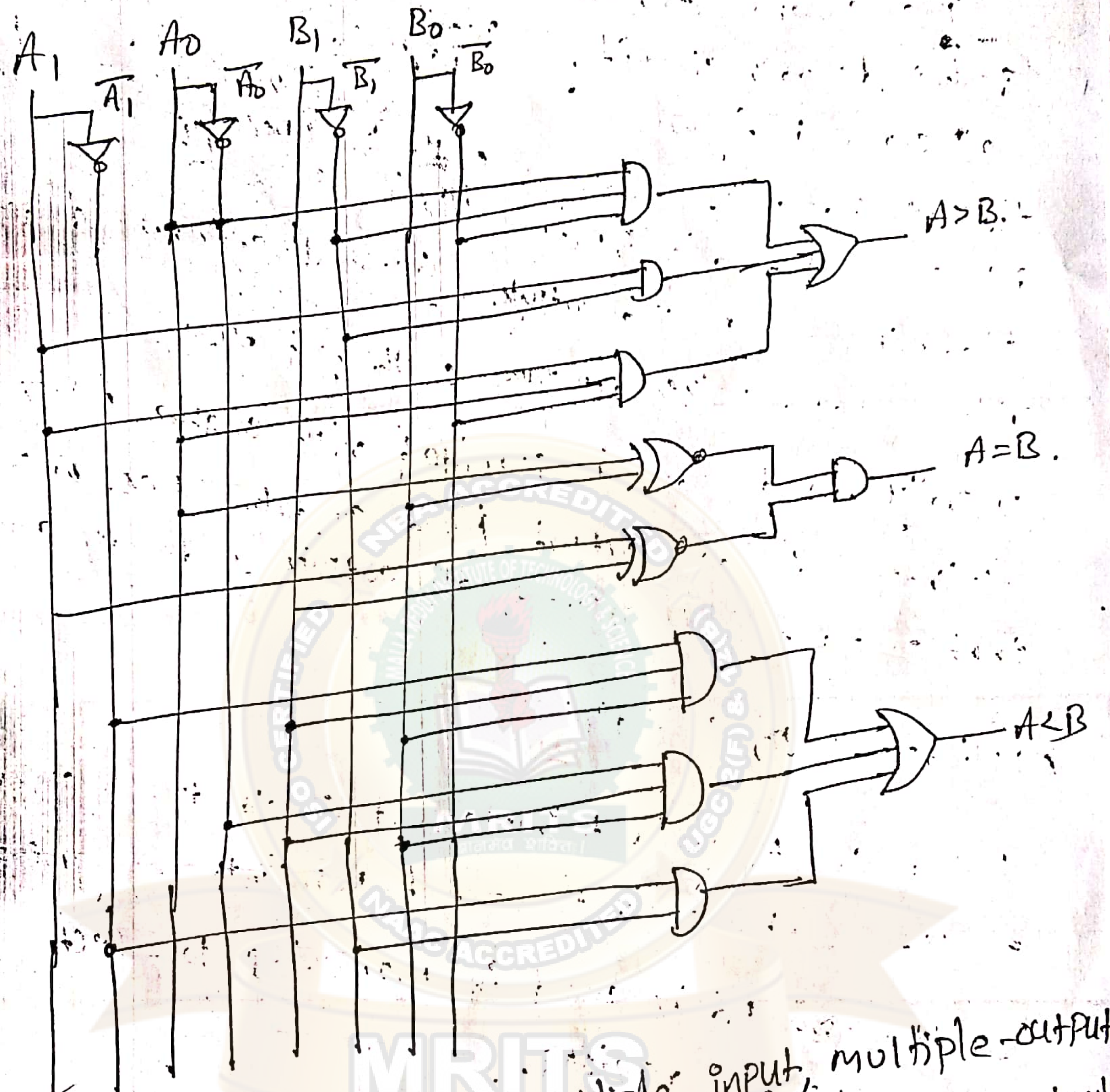
$= (A_0 \odot B_0)(A_1 \odot B_1)$

For $A<B$:-



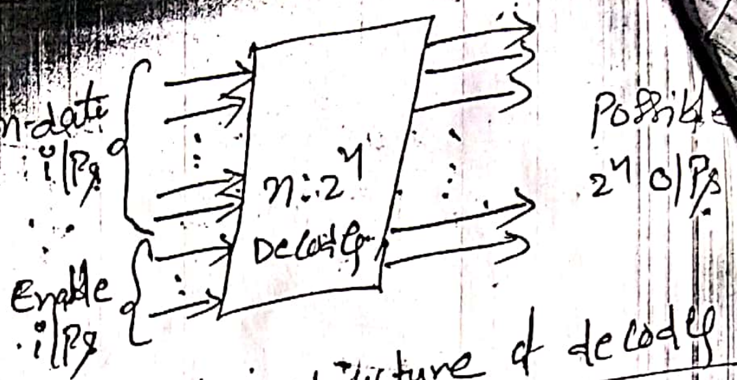
$A<B = \overline{A_1}\,\overline{A_1} B_0 + \overline{A_0} B_1 B_0 + \overline{A_1} B_1$

diagram :-



Decoders :- A decoder is a multiple-input, multiple-output logic circuit which converts coded inputs into coded outputs, where the input & output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word, i.e., there is one-to-one mapping from input code words into output code words. This one-to-one mapping can be expressed in a truth table.

The general structure of the decoder circuit as shown in figure,



General structure of decoder

The encoded information is presented as 'n' inputs producing 2^n possible outputs.
The 2^n output values are from 0 through 2^n-1.
Usually, a decoder is provided with enable inputs to activate decoded output based on data inputs. When any one enable input is unasserted, all outputs of decoder are disabled.

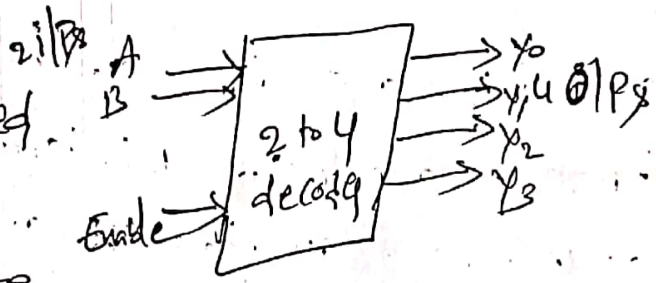
Applications of Decoder:-

1. It can be used to implement combinational circuit.
2. It can be used to convert BCD into 7-segment code.
3. It is used in memories to select particular register.

Binary Decoder:- A decoder which has an n-bit binary input code & a one activated output out of 2^n output code is called binary decoder. A binary decoder is used when it is necessary to activate exactly one of 2^n o/Ps based on an n-bit input value. It is similar to demultiplexer, with only one exception that it has no data input.

2 to 4 Decoder:

Here, 2-i/ps are decoded into 4-o/ps, each o/p representing one of the minterms of the 2-i/p variables.

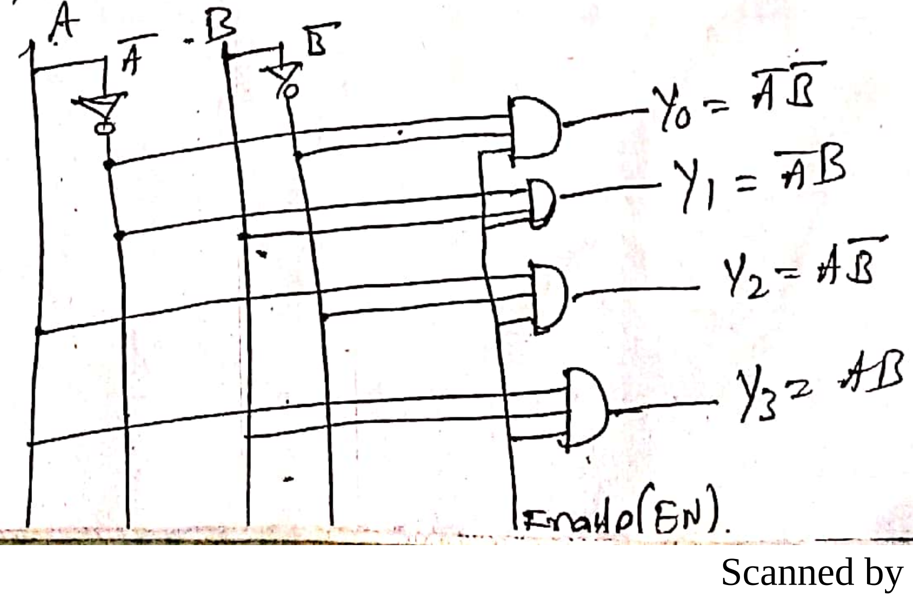


The two inverters provide the complement of the inputs, & each one of four AND gates generates one of the minterms

The truth table for a 2 to 4 decoder is shown below

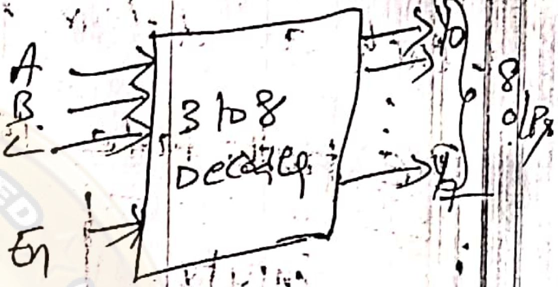
Inputs			Outputs			
EN	A	B	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

If enable i/p is 1 (EN=1), one & only one of the o/ps Y_0 to Y_3, is active for a given i/p. The o/p Y_0 is active. i.e. $Y_0=1$ when i/ps $A=B=0$, the o/p Y_1 is the active when i/ps $A=0$ & $B=1$. If enable i/p is 0 i.e. $EN=0$, then all the outputs are 0.



3 to 8 Decoder:-

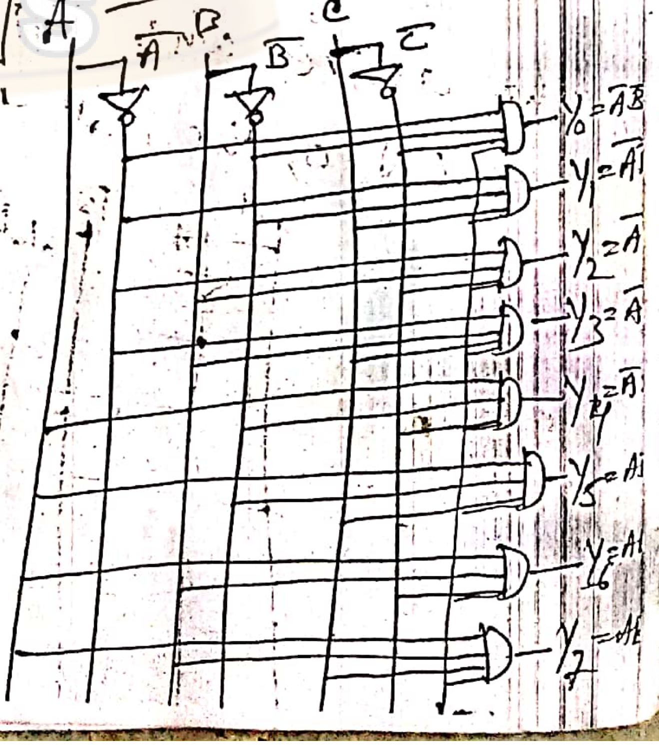
There are 3 i/ps are decoded into eight o/ps, each o/p represent one of the minterms of the 3 i/p variables. The three inverters provide the complement of the i/ps & each one of the eight AND gates generate one of the minterms. Enable input is provided to active decoded output based on data inputs A, B & C.



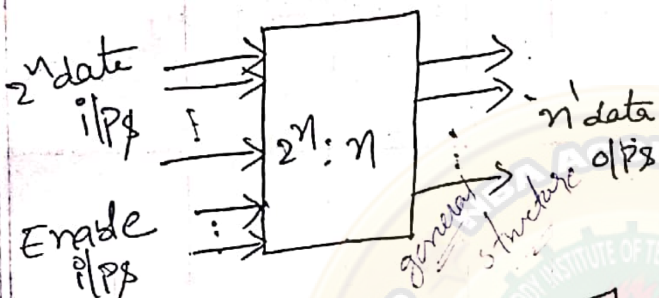
Truth table

i/ps				o/ps							
En	A	B	C	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

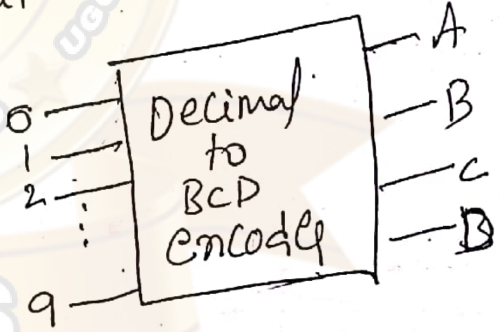
logic diagram



Encoders:- An Encoder is a digital circuit that performs the Inverse operation of a decoder. An encoder has 2^n i/p Lines & n o/p lines. In encoder, the o/p lines generate the binary code corresponding to the i/p value. The general structure of the encoder circuit is shown in figure. The decoded information is presented as 2^n i/ps producing 'n' (encoded) possible o/ps.



Decimal to BCD Encoder:- The decimal to BCD encoder, usually has ten input lines & four output lines. The decoded decimal data acts as an input for encoder & encoded BCD output is available on the four output lines.



i/p	o/ps			
	A	B	C	D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

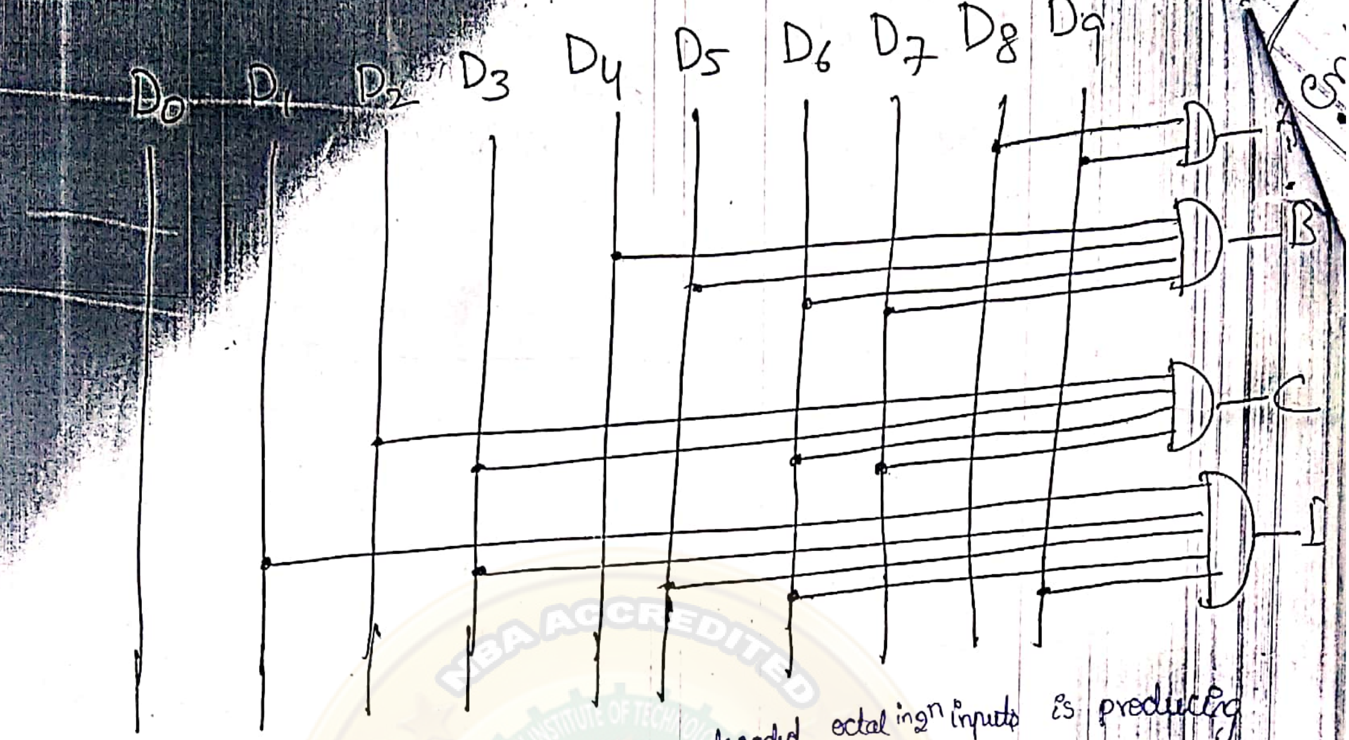
$A = D_8 + D_9$

$B = D_4 + D_5 + D_6 + D_7$

$C = D_2 + D_3 + D_6 + D_7$

$D = D_1 + D_3 + D_5 + D_7 + D_9$

Logic diagram for Decimal to BCD encoder:

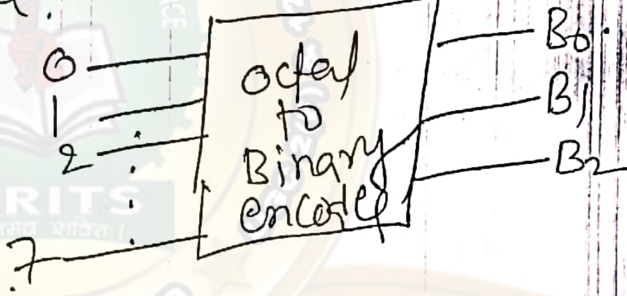


octal to Binary Encoder:

decoded octal ing^n inputs is producing encoded n-Binary outputs.

8-i/p lines &

3-o/p Lines



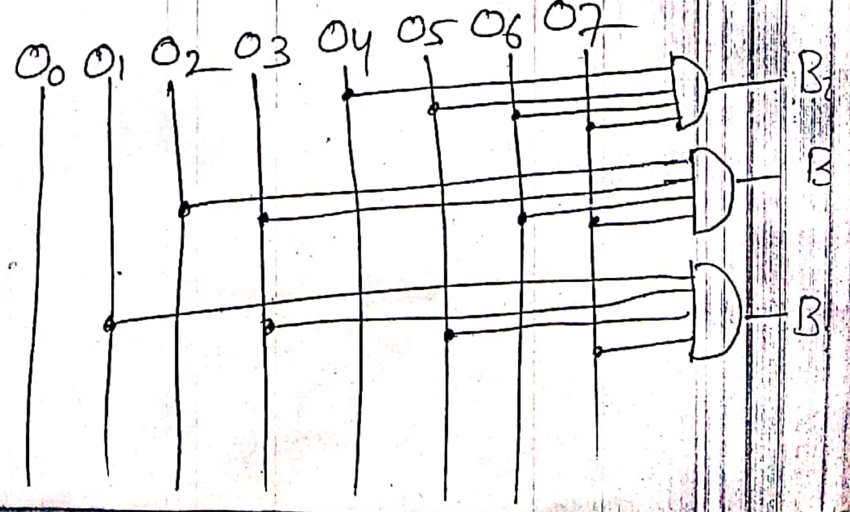
i/p	o/ps		
0	B_0	B_1	B_2
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

logic diagram

$B_0 = O_4 + O_5 + O_6 + O_7$

$B_1 = O_2 + O_3 + O_6 + O_7$

$B_2 = O_1 + O_3 + O_5 + O_7$



Priority Encoder:- A Priority encoder is an encoder circuit that includes the priority function. In priority encoder, if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

The truth table of 4-bit Priority encoder.

Inputs				outputs		
I_0	I_1	I_2	I_3	Y_1	Y_0	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

I_4 truth table, shows I_3 i/p with highest priority & I_0 i/p with lowest priority. when I_3 i/p is high, regradless of other i/ps output is 11. The I_2 has the next priority is 10 generated only if higher priority

The o/p for I_1 is i/ps are 01, & so on. The o/p V (a valid o/p indicator) indicates 1, one or more of the inputs are equal to 1. if all i/ps are 0, V is equal to 0.

K-map simplification

For Y_1, Y_0 & V.

For Y_1:

I_0I_1 \ I_2I_3	00	01	11	10
00	X	1	1	1
01	0	1	1	1
11	0	1	1	1
10	0	1	1	1

$I_3 + I_2$

$Y_1 = I_2 + I_3.$

For Y_0: I_3 LSB

I_0I_1 \ I_2I_3	00	01	11	10
00	X	1	0/1 X	0
01	1	1	1 0 X	0
11	1	1	0 X	0
10	0	1	X	0

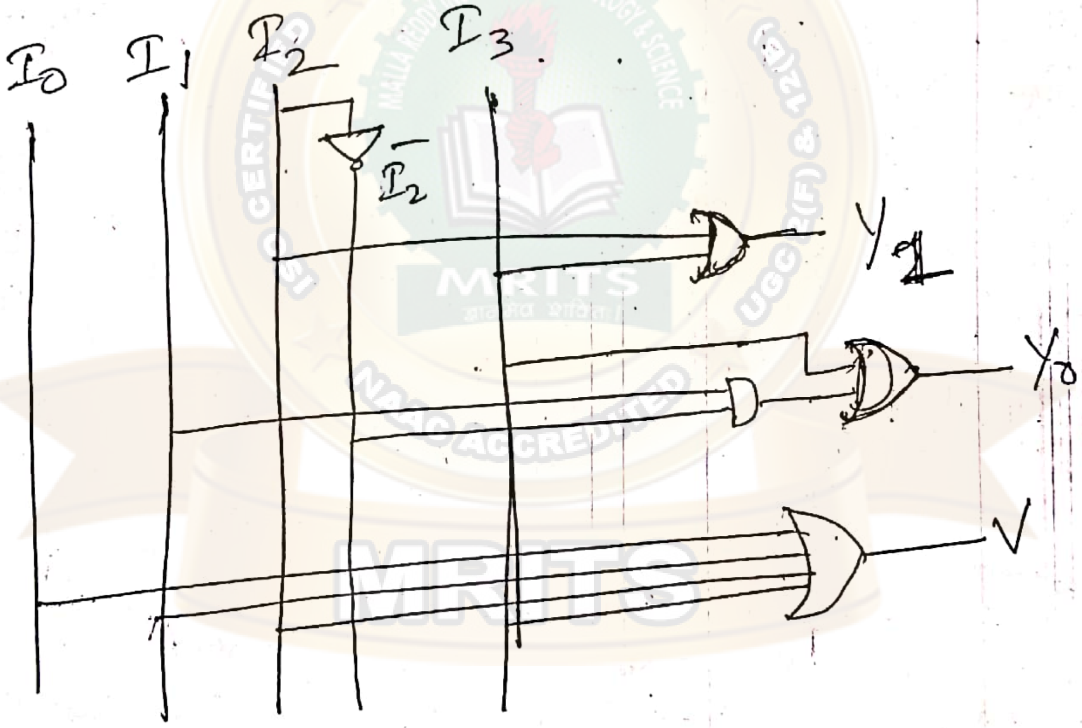
$Y_0 = I_3 + I_1 \bar{I}_2$

For V:

I_0I_1 \ I_2I_3	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$V = I_0 + I_1 + I_2 ...$

Logic Diagram:



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Multiplexers :- 2m

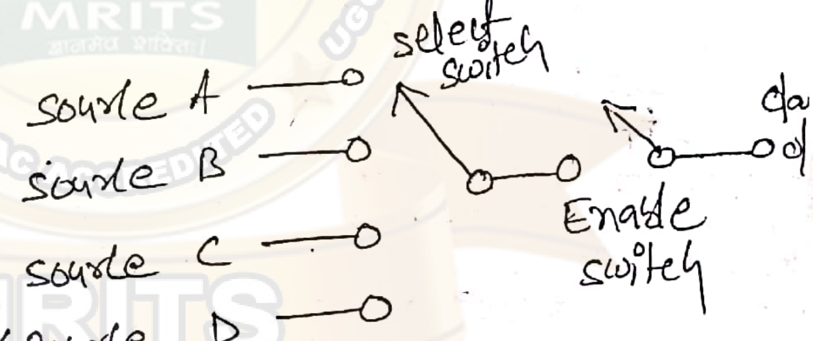
It is Combinational circuit that selects binary information from one of many input lines & directs it to one o/p line.

Multiplexer is a digital switch.

The basic multiplexer has several data-input lines & a single o/p line. The selection of a particular i/p line is controlled by a set of selection lines.

→ Normally, there are n i/p lines & 2^m selection lines whose bit combinations determine which i/p is selected.

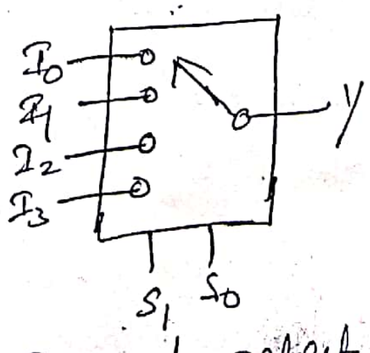
→ Therefore, multiplexer is "many into one".

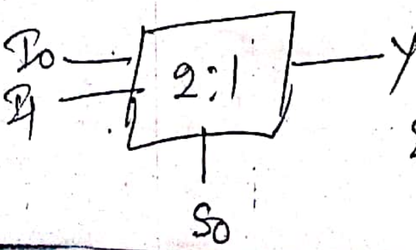


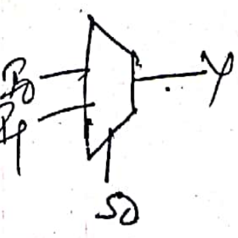
Analog selector switch

Advantages :-

- Reduces no of wires
- Reduces ckt complexity & cost.
- Implementation of various ckt using MUX







$(n) = 2^{(m)}$ m → no of select lines

$m = \log_2 n$

Ex:- n = 4

$m = \log_2 n = \log_2 2^2$

$= 2 \log_2 2$

$m = 2 \cdot 1 = 2$

Types:-

1) 2:1 MUX 2) 4:1 MUX 3) 8:1 MUX 4) 16:1 MUX &

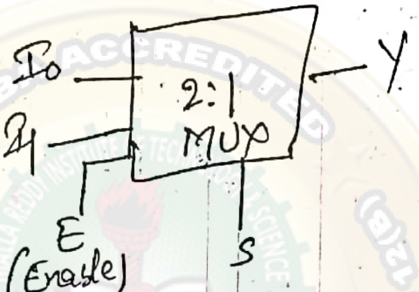
5) 32:1 MUX

1) 2:1 MUX:-

no. of i/ps - 2

o/p - 1

selection line - 1

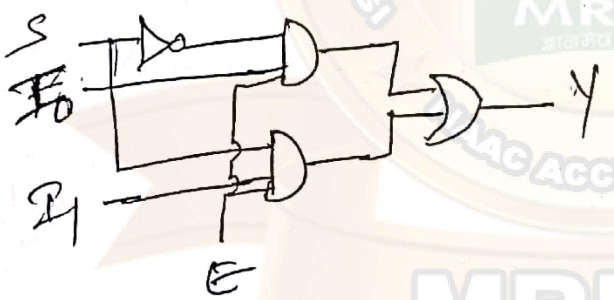


E	S	Y
0	X	0
1	0	I_0
1	1	I_1

not wo

$Y = E \cdot \bar{S} I_0 + E \cdot S \cdot I_1$

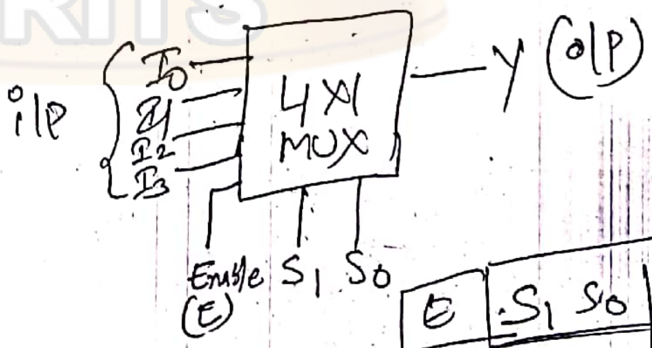
$Y = E(\bar{S} \cdot I_0 + S \cdot I_1)$



	S_0	S_1
	0	1
E 0		
E 1	I_0	I_1

$Y = E(\bar{S} I_0 + S I_1)$

4x1 Multiplexer



n = 4

$m = \log_2 n$

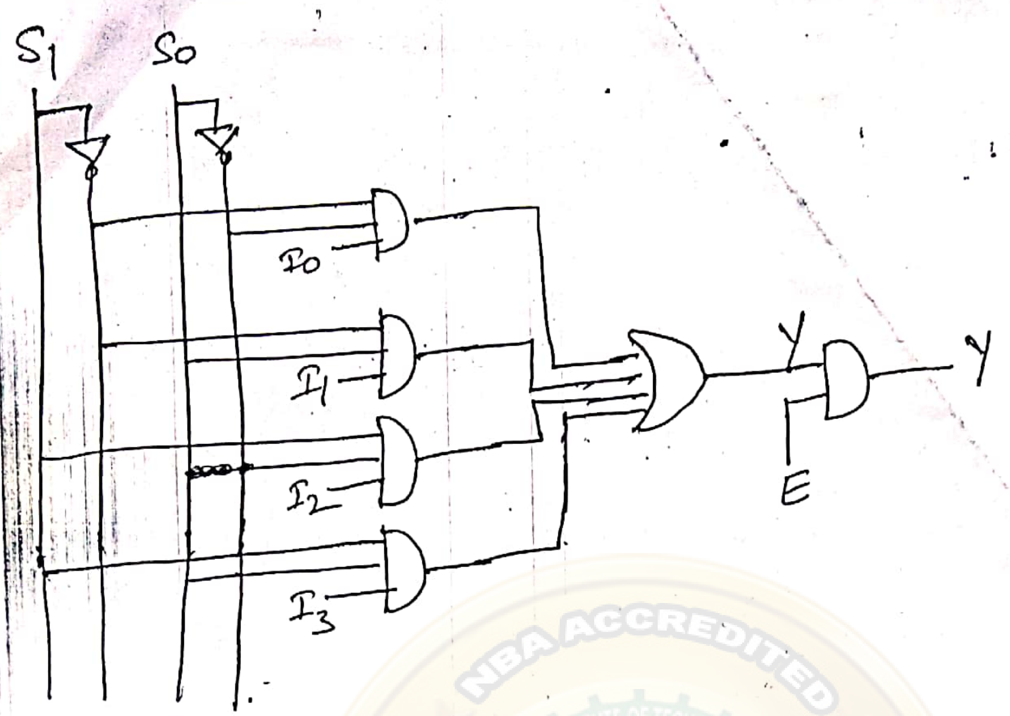
$= \log_2 4 = \log_2 2^2$

selection lines (m) $= 2 \log_2 2 = 2 \cdot 1 = 2$

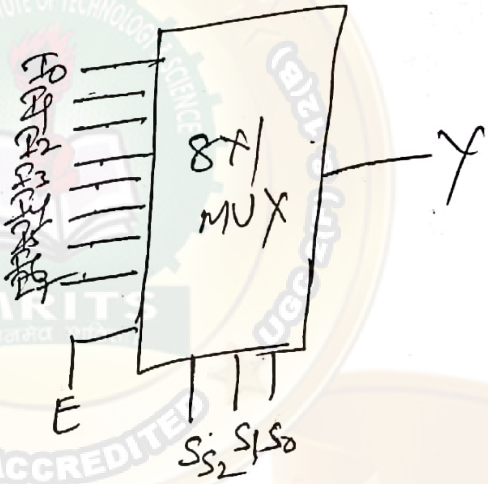
$Y = \bar{S_1} \bar{S_0} I_0 + \bar{S_1} S_0 I_1 + S_1 \bar{S_0} I_2 + S_1 S_0 I_3$

E	S_1	S_0	Y
1	0	0	I_0
1	0	1	I_1
1	1	0	I_2
1	1	1	I_3
0	X	X	0

Logic diagram:



8X1 MUX:



$n = 8 = 2^3$

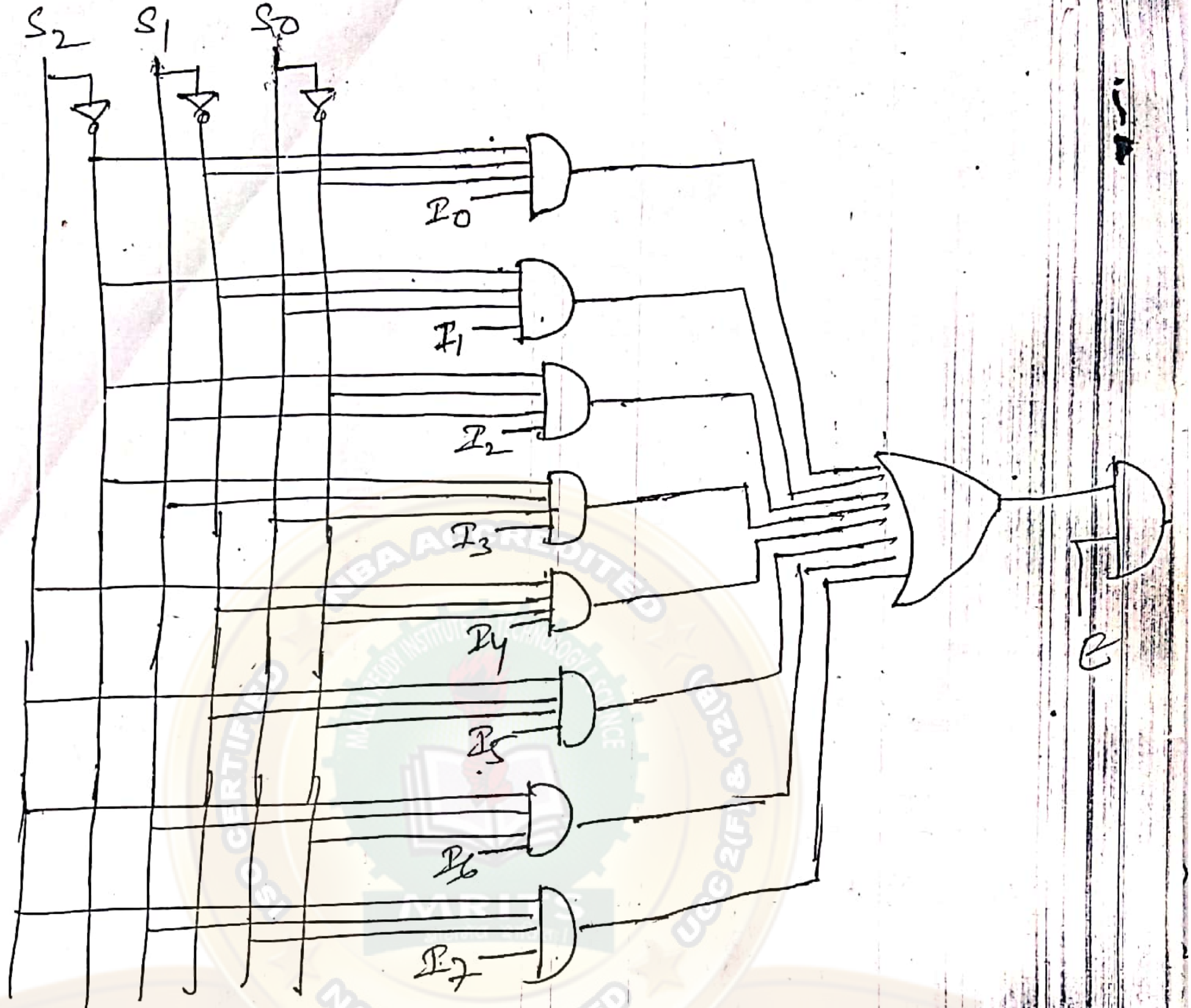
$M = \log_2 n = \log_2 2^3$

$= 3 \log_2 2 = 3 \cdot 1 = 3$

E	S_2	S_1	S_0	Y
	0	0	0	I_0
	0	0	1	I_1
	0	1	0	I_2
	0	1	1	I_3
	1	0	0	I_4
	1	0	1	I_5
	1	1	0	I_6
	1	1	1	I_7
0	X	X	X	0

$$Y = \bar{S_2}\bar{S_1}\bar{S_0} I_0 + \bar{S_2}\bar{S_1} S_0 I_1 + \bar{S_2} S_1 \bar{S_0} I_2 + S_2 \bar{S_1}\bar{S_0} I_4 + S_2 \bar{S_1} S_0 I_5 + \bar{S_2} S_1 S_0 I_3 + S_2 S_1 \bar{S_0} I_6 + S_2 S_1 S_0 I_7$$

Logic diagram:



Applications of multiplexers:

1. They are used as a data selector to select one out of many data i/ps
2. They can be used to implement combinational logic ckt
3. They are used in time multiplexing systems
4. They are used in frequency multiplexing systems
5. They are used in A/D & D/A converters
6. They are used in data acquisition systems.

1

Unit-5

Sequential Logic Circuits

⇒ **Sequential Logic Circuit :-**

In sequential circuit, the output depend not only on the present inputs but also on the sequence of all the past inputs. i.e. previous ~~state~~ o/p state of the circuit.

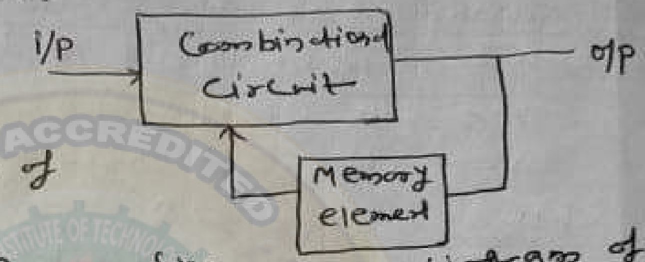


fig: Block diagram of sequential circuit.

→ Sequential circuits require memory elements to store the previous output or state of the machine to determine the present output.

→ A sequential circuit can be classified into synchronous and Asynchronous circuits.

(i) **Synchronous sequential circuit :-**
If the transitions of the sequential circuit from one state to the next state are controlled by a clock, then the circuit is called a synchronous sequential circuit.

(ii) **Asynchronous sequential circuit :-**
When the circuit is not controlled by a clock, ~~then the circuit~~ transition from one state to the next state occurs whenever there is a change in the input to the circuit at any time, this circuit is called as asynchronous sequential circuit.

→ Asynchronous sequential circuit give high speeds.

Asynchronous sequential circuit are also classified into fundamental mode asynchronous sequential circuits and pulse mode asynchronous sequential circuits.

→ If the number of state variable is 'n' then the sequential circuit has 2n possible states.

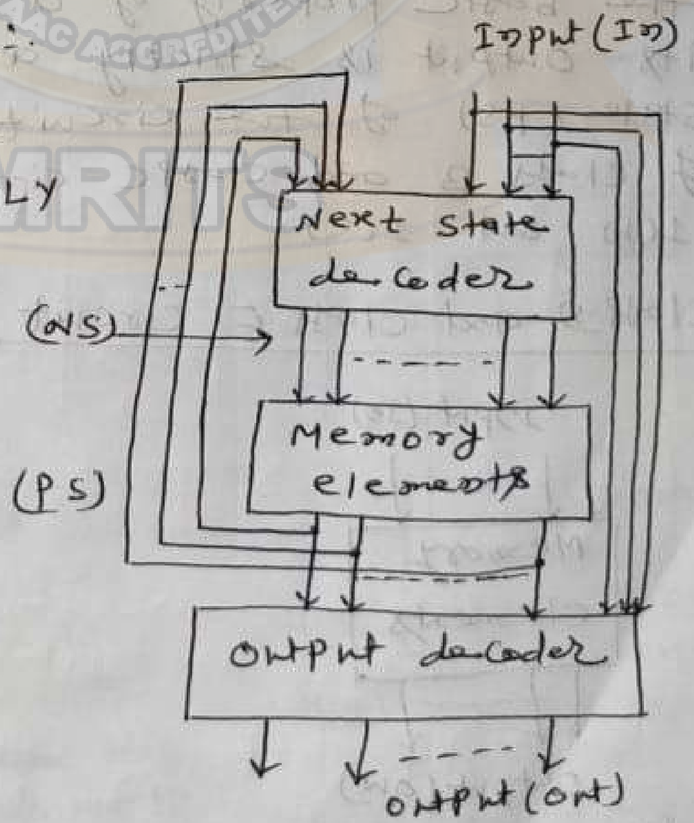
⇒ Classification of Sequential Circuits:-

Sequential circuits are generally classified into five different classes:

(i) Class A circuit
(ii) Class B circuit
(iii) Class C circuit
(iv) Class D circuit
(v) Class E circuit

(I) Class A circuit:-

The Class A circuit is defined as a MEALY circuit named after G.H Mealy. The basic property of Mealy circuit is that the o/p is a function of the present input condition and the present state (PS) of the circuit.



fig(1)(a) Class A circuit

Class B and class C circuits :-

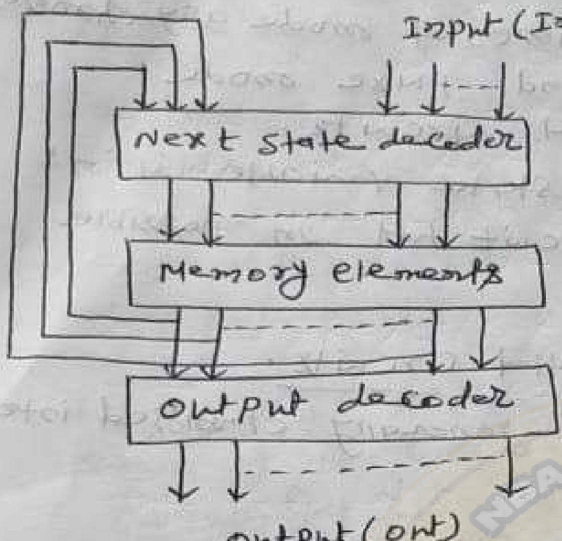


fig (1)(B) Class B circuit
(MOORE circuit)

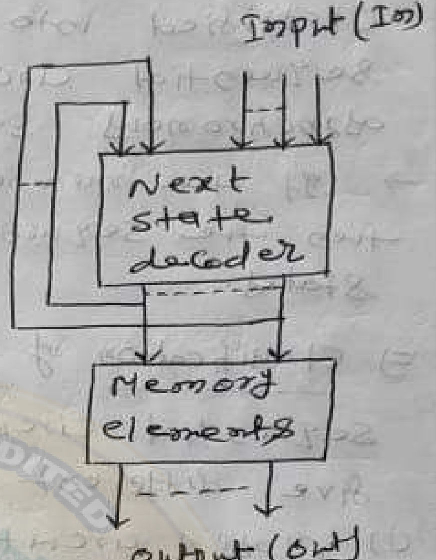
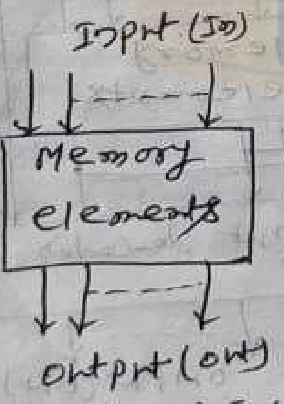


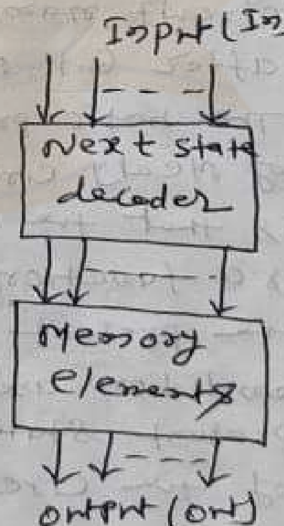
fig (1)(C) class C circuit

The class C and class B circuits are generally defined as MOORE circuit, named after E.F. moore. The basic property of a moore circuit is that its output is strictly a function of present state (PS) of the circuit inputs. The block diagram of class B and class C circuits are shown in fig 1(b) and 1(c).

class D and class E circuit :-



fig(d) class E circuit



fig(e) class D circuit

4

The block diagram connection for class D and class E circuits are shown in fig 1(d) and 1(e).

⇒ Latches :-

The basic unit of storage is the latch or flip-flop. This simplest kind of a sequential circuit has only two states. It is a memory cell, which is capable of storing one bit of information i.e. logic 1 or 0. This sequential circuit is also called a latch since one bit of information can be locked or latched. The basic latch consists of two inverters as shown in fig (a).

fig(a) basic latch - cross coupled inverters

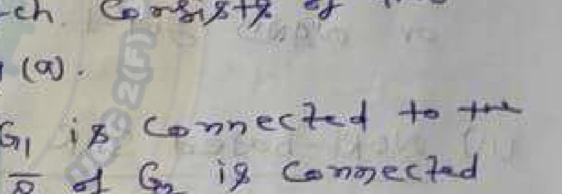
→ The output Q of inverter G_1 is connected to the input x_2 of G_2 and output $\bar{Q}$ of G_2 is connected to the input x_1 of G_1.

Let assume the output of G_1 i.e $Q_1 = 1$ ~~and~~ ~~output $\bar{Q}$ of G_2 is~~ then the output of G_2 i.e. $\bar{Q} = 0$

similarly, when $Q = 0$ then $\bar{Q} = 1$

→ If the circuit is in state 1 or 0 at Q and $\bar{Q}$ respectively, it continues to remain latched in the same state.

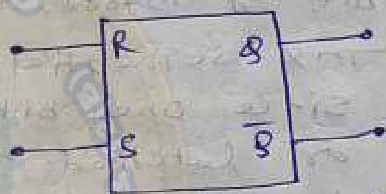
→ The general block schematic representation of a latch with provision to enter digital data is shown in fig(b). It has one or more input and two outputs Q and $\bar{Q}$. Two outputs are complement of each other.



fig(b) Block diagram of a latch with provision to enter digital data.

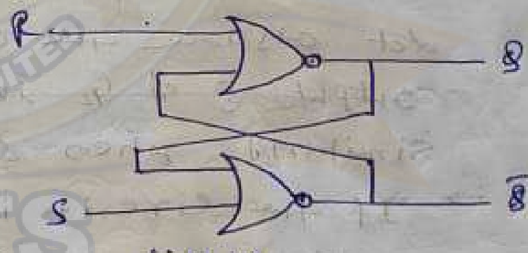
If $Q = 0$ → Reset then $\bar{Q} = 1$
If $Q = 1$ → Set then $\bar{Q} = 0$
When the latch output $Q = 0$ or 1, it will remain in the same state until one or more of the inputs are excited to effect a change in the output. Since the latch o/p will remain set/Reset until the trigger pulse is given to change the state.

(i) Set-Reset (S-R) Latch:
The S-R latch has two inputs namely SET (S) and RESET (R) and two outputs Q and $\bar{Q}$.
The S-R latch can be easily implemented using NOR gates or NAND gates.



fig(a) block diagram

(ii) NOR-based S-R latch:
The NOR-based S-R latch is shown in fig(b).



fig(b)

Truth table

Input		Output Q	$\bar{Q}$	Action
S	R	Q_n	Q_{n+1}	state
0	0	Q_n	Q_n	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	X	Forbidden → Invalid

Here,
Q_n → Represent the state of flip-flop before applying the input (i.e. present state)
Q_{n+1} → Represent the state of flipflop after the application of input (i.e. next state)

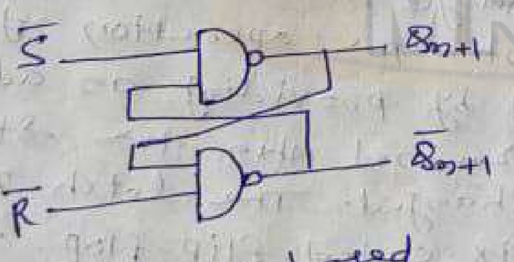
Case1 :- When S = 0 and R = 0,
This is the normal resting state of the NOR latch and it has no effect on the output state. Q and Q̄ will remain in same state as they are prior to the occurrence of this input condition

Case2 :- When S = 1 and R = 0
This will always set Q = 1, where it will remain even after set return to 0.

Case3 :- When S = 0 and R = 1
This will always Reset Q = 0, where it will remain even after RESET return to 0.

Case4 When R = 1 and S = 1
This condition tries to SET and RESET the latch at the same time and it produces $Q = \bar{Q} = 0$. If the inputs are return to zero simultaneously, the resulting output state is erratic and unpredictable. This input condition should not be used. It is forbidden.

(iii) NAND - based $\bar{S}$-$\bar{R}$ latch (Active-low SR Latch) :-



fig(a) NAND based SR Latch

Input		Output		Action
$\bar{S}$	$\bar{R}$	Q_{n+1}	$\bar{Q}_{n+1}$	State
0	0	x	x	forbidden
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q_n	$\bar{Q}_n$	No change

fig(b) Truth table

The NAND based $\bar{S}$$\bar{R}$ Latch is shown in fig(a). ... any input of a NAND gate will force ... high. The truth table of NAND-based is ...

$\bar{S}\,\bar{R}$ latch is shown in table (b).

Case 1 :- When $\bar{S} = 0$ and $\bar{R} = 0$.
i.e. when both inputs go to 0, both output go to 1.
i.e. $Q_{n+1} = 1$ and $\bar{Q}_{n+1} = 1$.
This condition is ambiguous and should not be used.

Case 2 :- When $\bar{S} = 0$ and $\bar{R} = 1$, always produces $Q_{n+1} = 1$ regardless of the present state of the latch output.
This condition is set.
i.e. $Q_{n+1} = 1$ and $\bar{Q}_{n+1} = 0$

Case 3 :- When $\bar{S} = 1$ and $\bar{R} = 0$ forces the lower NAND gate output to 1. i.e. $\bar{Q}_{n+1} = 1$. Since the inputs of upper NAND gates are now, both the inputs of upper NAND 1 and therefore the output of upper NAND gate is low. i.e. $Q_{n+1} = 0$ regardless the prior state of the latch.
This condition is Reset (clear) the latch.

Case 4 :- When $\bar{S} = 1$ and $\bar{R} = 1$ does not affect the state of the latch. It remains in its prior state.

⇒ Flip-flop :-
Synchronous circuits change their states only when clock pulses are present. The operation of the basic can be modified by providing an additional control input that determines when the state of the circuit is to be changed. The latch with the additional control input is called flip-flop. The additional control input is either the clock or enable input.

There are four basic types of flip-flop :-
① S-R flip flop,
② JK - flip flop
③ D - flip flop
(4) T - flip flop

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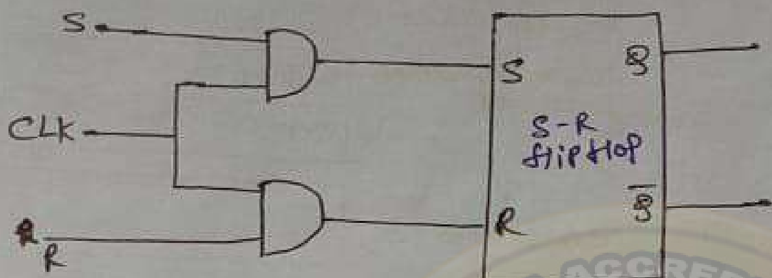
S-R flip-flop:-

The S-R flip-flop consist of two additional AND gate at the S and R inputs of S-R latch as shown in fig(a).



fig(a) Block diagram of S-R flipflop

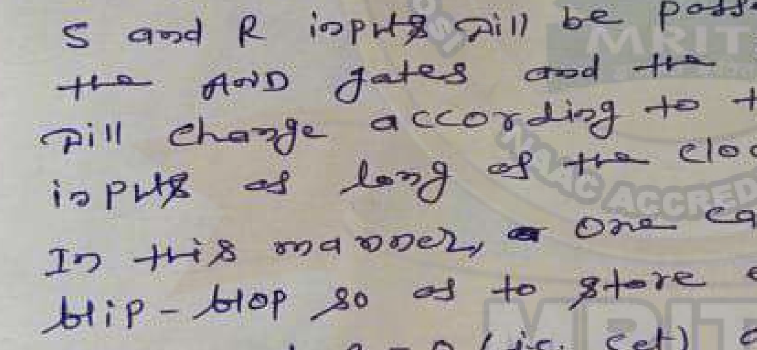
→ In this circuit, when the clock input is Low, the output of both the AND gates are LOW and the changes in S and R will not affect the output Q of the flip-flop.

→ When the clock input is HIGH, the value at S and R inputs will be passed to the output of the AND gates and the output Q of the flip-flop will change according to the changes in S and R inputs as long as the clock input is HIGH.

In this manner, one can strobe or clock the flip-flop so as to store either a 1 by applying S = 1 and R = 0 (i.e. Set) or a 0 by applying S = 0 and R = 1 (i.e. Reset) at any time.

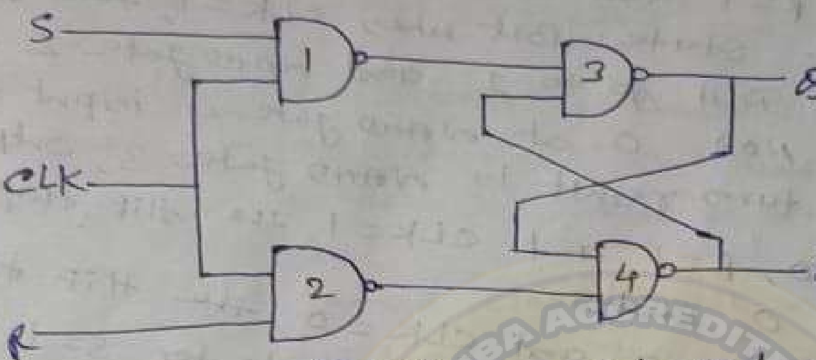
This flip-flop is called clocked S-R flip-flop.

→ The S-R flip-flop which consists of the basic NOR latch and two AND gates is shown in fig(b).



fig(b) clocked NOR based S-R flipflop

→ The S-R flip flop which consist of basic NAND latch and two other NAND gates is shown in fig(c).



fig(c) NAND based S-R flip flop

fig(d) Graphic Symbol

→ The truth table of S-R flipflop:-

Present state (Q_n)	CLK pulse (CLK)	Data I/P S	R	Next State Q_{n+1}	Action
0	0	0	0	0	No change
1	0	0	0	1	No change
0	1	0	0	0	No change
1	1	0	0	1	No change
0	0	0	1	0	No change
1	0	0	1	1	No change
0	1	0	1	0	Reset
1	1	0	1	0	Reset
0	1	1	0	1	Set
1	1	1	0	1	Set
0	1	1	1	×	forbidden
1	1	1	1	×	forbidden.

Case 1:- For S = 0, R = 0 and CLK = 0, the flip flop remains in its present state. i.e. Q remains unchanged. Even for S = 0, R = 0 and CLK = 1, the flip flop remains in its present state. The first

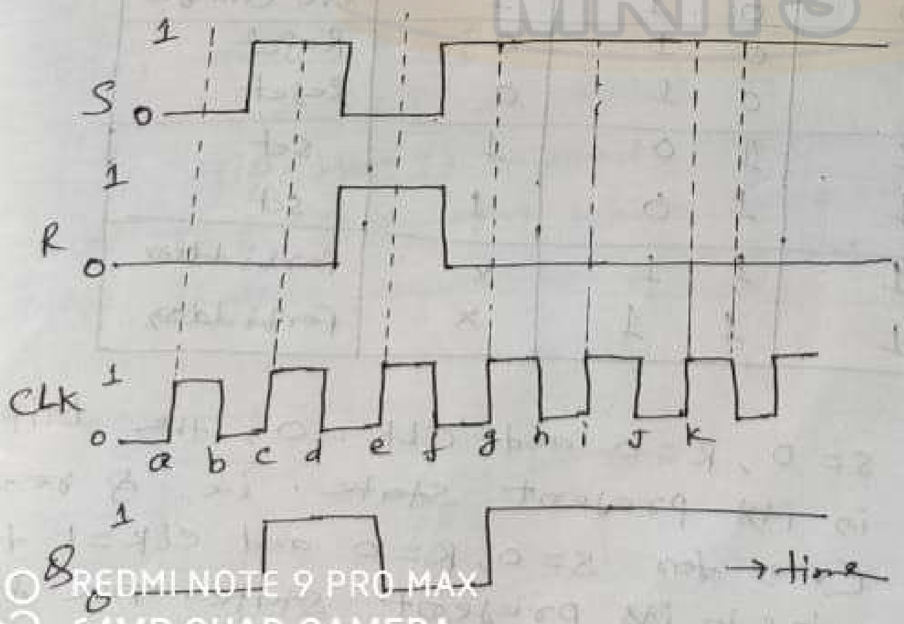
four rows of the truth table clearly indicate that the state of the flip-flop remains unchanged.
i.e. $Q_{n+1} = Q_n$.

Case 2 :- for S=0, R=1 and CLK=0, the flip flop remains in its present state. But when CLK=1, the NAND gate-1 output will go to 1 and NAND gate-2 output will go to 0. Now, 0 at NAND gate-4 input forces $\bar{Q}=1$ which in turn result in NAND gate-3, output Q=0. Thus for S=0, R=1 and CLK=1, the flip-flop RESET to the 0 state.

Case 3 :- for S=1, R=0 and CLK=0, the flip-flop remains in its present state. But for S=1, R=0 and CLK=1, the set state of flip-flop is reached. This causes the NAND-gate 1 output to go to 0 and the NAND-gate 2 output to 1. Now, 0 at NAND gate-3 input forces Q to 1 which in turn forces NAND gate-4 output $\bar{Q}$ to 0.

Case 4 :- An intermediate condition occur when all the inputs i.e. CLK, S and R are equal to 1.

→ The operation of S-R flip-flop is illustrate by the waveform as shown in fig(E).



fig(E) waveform of S-R flip-flop

(i) Initially all inputs are 0 and the Q output is 0.

(ii) When the rising edge of the first clock pulse occurs (point a), the S and R inputs are both 0, so the flip-flop is not affected and it remains in the Q = 0 state.

(iii) At the occurrence of the rising edge of the second clock pulse (point c), S=1 and R=0. Thus, the flip-flop sets to the 1 state at the rising edge of this clock pulse.

(iv) When the third clock pulse makes its positive transition (point e), it finds that S=0 and R=1, which causes the flip-flop to reset to the 0 state.

(v) The fourth pulse sets the flip-flop once again to the Q=1 state (point g), because S=1 and R=0 when its positive edge occur.

(vi) The fifth pulse finds that S=1 and R=0, when its makes its positive going transition. However Q is already high, so it remains in that state.

(vii) The R=1 and S=1 condition should not be used as it results in an indeterminate condition.

⇒ D-flip-flop (Delay-flip-flop):

The D flip flop has only one input called the delay (D) input and two outputs Q and $\bar{Q}$. D-flip-flop can be constructed from an S-R flip-flop by inserting an inverter between S and R and assigning the symbol D to the S input. D-flip-flop is shown in fig.

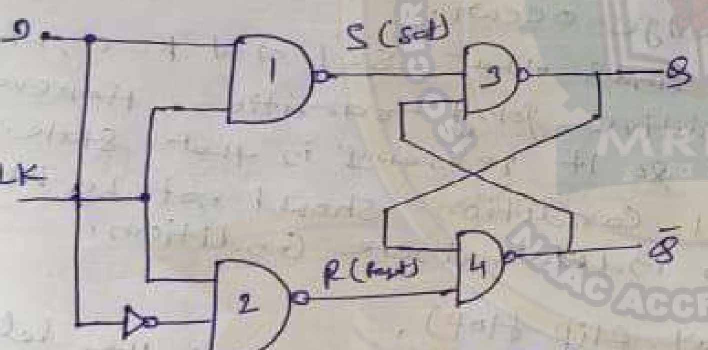
→ It operates as follows:-

1. When the CLK input is LOW, the D input has no effect, since the set and reset inputs of NAND flip-flop are kept High.

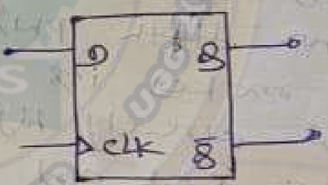
2. When the clock goes HIGH, the Q output will take on the value of the D input. If

CLK = 1 and D=1, the NAND gate-1 output goes 1 which is $\bar{S}$ input of the basic NAND based S-R flip-flop and NAND gate-2 output goes 1 which is the R input of the basic NAND-based S-R flipflop. Therefore, for $\bar{S}=0$ and $\bar{R}=1$, the flip flop output will be 1, i.e. it follows D input.
Similarly, for CLK=1 and D=0, the flip flop output will be 0. If D changes while the CLK is HIGH Q will follow and change quickly.

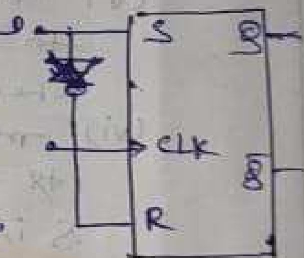
→ As transfer of data from the input to the output is delayed, it is known as delay (D) flip-flop. The D-type flip-flop is either used as a delay or as a latch to store 1 bit of binary information.



fig(a) D-flip flop using NAND gates



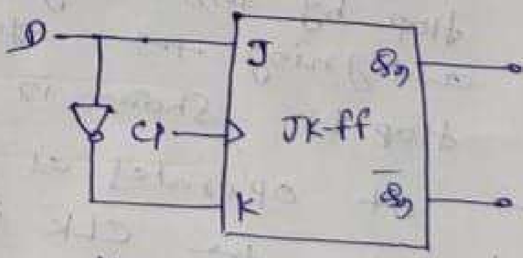
fig(b) Logic Symbol



fig(c) D-flip flop using S-R flipflop

→ Truth table of D-flip-flops.

CLK	Input D	Output Q_{n+1}
1	0	0
1	1	1
0	X	No change

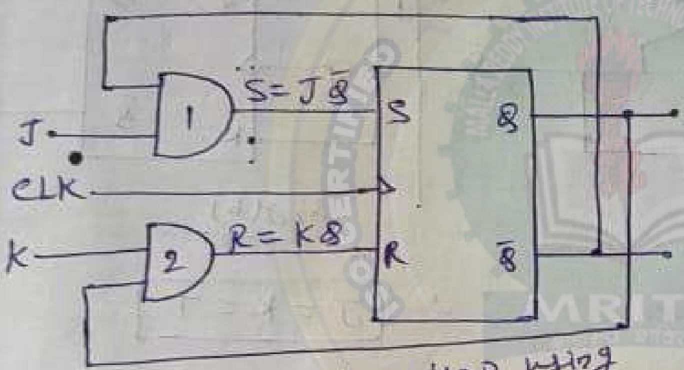


fig(d) D-flipflop using J-K flip-flop.

J = D and K = $\bar{D}$

J-K flip flop.

A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting two AND gates as shown in fig (a). The data input J and the output $\overline{Q}$ are applied to the first AND gate, and its output ($J\overline{Q}$) is applied to the S input of S-R flipflop. Similarly, the data input K and output Q are connected to the second AND gate and its output (KQ) is applied to R input of S-R flip flop. The graphic symbol of J-K flip flop is shown in fig (b).



fig(a) J-K flip flop using S-R flip flop

fig(b) Graphic symbol of J-K flipflop

$$\therefore \quad S = J\overline{Q}, \text{ and } R = KQ$$

Truth table of J-K flip-flop.

Clock	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	HOLD
1	0	1	0	Reset
1	1	0	1	SET
1	1	1	$\overline{Q_n}$	Toggle state

characteristics table

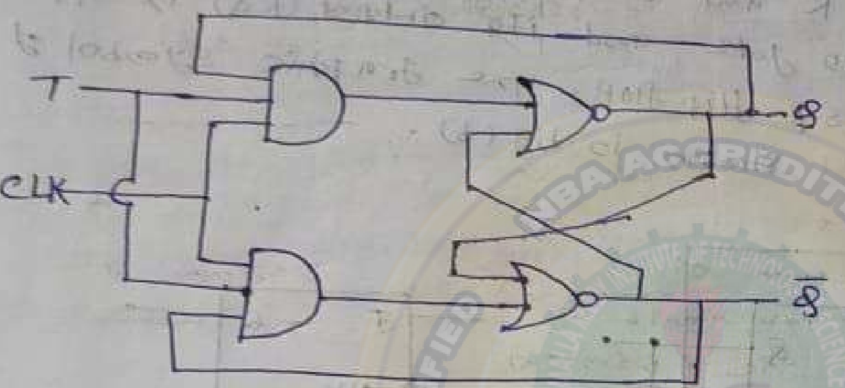
J	K	Q_n	Q_{n+1}	
0	0	0	0	→ Q_n
0	0	1	1	
0	1	0	0	→ 0
0	1	1	0	
1	0	0	1	→ 1
1	0	1	1	
1	1	0	1	→ $\overline{Q_n}$
1	1	1	0	

∴ characteristics Eqn is

$$Q_{n+1} = J\overline{Q_n} + \overline{K}Q_n$$

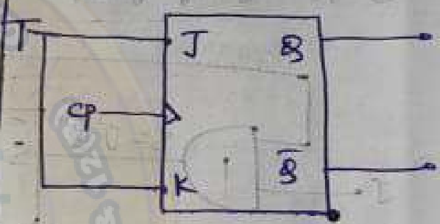
Toggle flip-flop (T-ff).

- → The T-ff is a single input version of the J-K ff.
- → T-ff can be obtained from a J-K ff if J and K are tied together as shown in fig(a).
- → The designation 'T' comes from the ability of the ff to "toggle" or change state.



fig(a)

Graphical symbol of T-ff



fig(b)

$J = K = T$

Truth table of T-ff

CLK	T	Q_{n+1}
0	X	Q_n
1	0	Q_n → Hold state
1	1	$\bar{Q}_n$ → Toggle state

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Characteristics Eq^n is

$$Q_{n+1} = \bar{T} Q_n + T \bar{Q}_n = T \oplus Q_n$$

⇒ Race-Around Condition :-

→ The Race-around Condition will occur when

(i) $J = K = 1$

(ii) $t_{pd(FF)} < t_{pw}$

(iii) flip-flop is level triggered.

→ For the duration 't_{pd}' of the clock pulse, the output Q will oscillate back and forth between 0 and 1. At the end of the clock pulse, the value 'Q' is uncertain. This situation is reffered as race around condition.

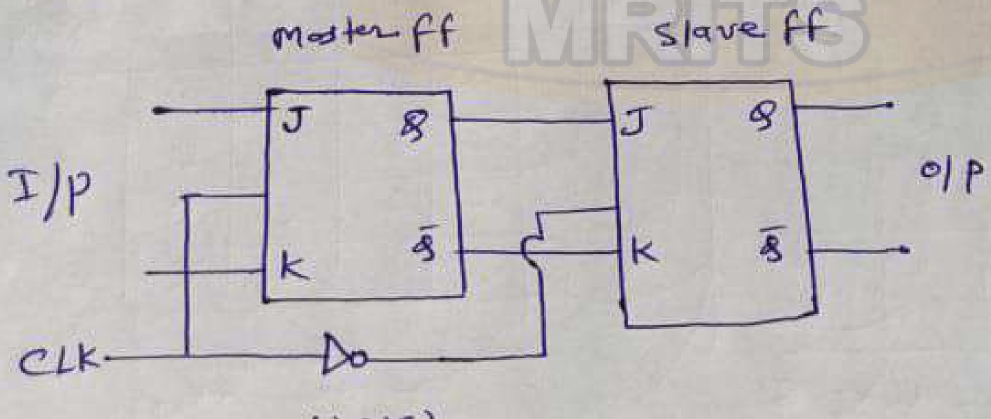
→ To avoid race-around condition,

$$t_{pw} < t_{pd(ff)} < T$$

→ Race around condition does not occur in edge triggered flip-flop.

⇒ Master-slave J-K flip-flop :-

To avoid race-around condition, master slave ff is used.



fig(a)

→ In master slave flip flop, master is applied with input clock and slave is applied with inverted clock. The ... is when master output is changing slave output remains in previous state.

→ In master slave flip-flop, output will change only when slave output changes.

→ Output of master can change many times but slave output can change only one time so master ff act as level triggered and slave ff act as edge triggered. Therefore, there is no race around condition at the output of the slave.

⇒ Shift Register :-

→ A register is used to store binary information is known as a memory register. A register capable of shifting binary information either to the right or to the left is called a shift register.

→ In register to store n-bit, it required n-ff.

→ There are two methods of shifting the data.
(i) serial shifting and (ii) parallel shifting.

→ Depending upon input and output, registers can be classified into 4 types:-

(a) SISO – Serial In Serial Out
(b) SIPO – Serial In parallel Out
(c) PISO – parallel In Serial Out
(d) PIPO – parallel In parallel Out

(a) SISO (Serial-In-Serial Out) :-

(i) 4-bit Right-shift SISO Register :-

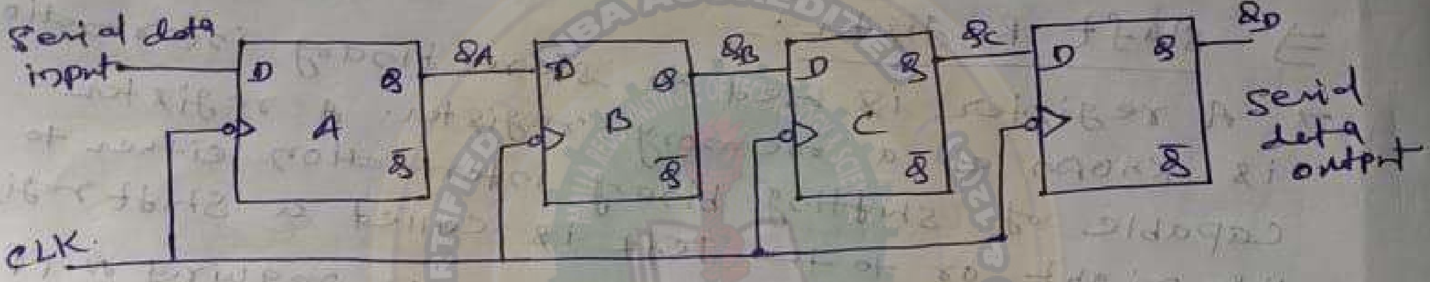
→ In right shift SISO register, LSB data is applied at the MSB ff (D-ff)

→ In 'n' bit register, to enter 'n' bit data, it required 'n' clock pulses in serial form.

→ If 'n' bit data is stored in SISO register then output is taken serially for this (n-1) clock pulses are required.

→ SISO register is used to provide 'n' clock pulse delay to the input data.

→ If 'T' is the time period of clock pulse, then delay provided by SISO is nT.



Let us consider 1101 data is entered. The truth table-1 shows the operation of entry of 1101. Truth table-2 shows the action of shifting all logical-1 inputs into an initially reset shift register.

Shift pulse	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	0	1	0
4	1	1	0	1

Truth table-1.

Shift pulse	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1

Truth-table-2

(ii) 4-bit Left shift SISO register.

→ In Left shift SISO register, MSB data is applied to the LSB ff (D ff).

→ To enter the 'n' bit data in serial form we require 'n' clock pulse. 18

→ To exit or getting output of 'n' bit data of serially we require (n-1) clock pulse.

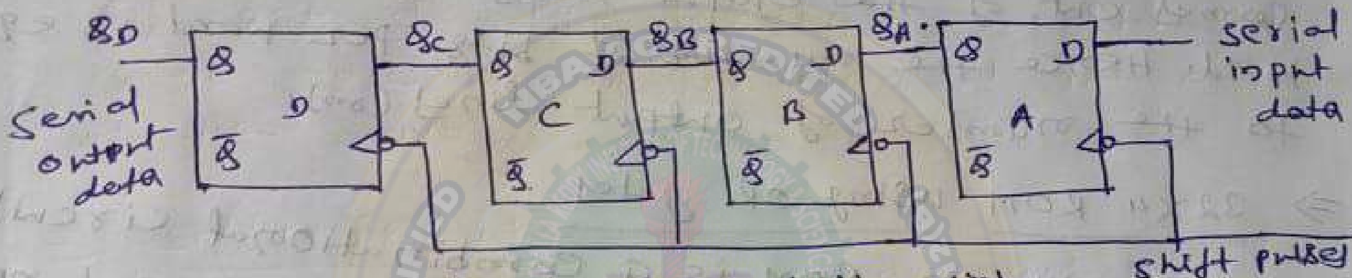


fig (a) Shift left register.

Shift pulse	QD	QC	QB	QA

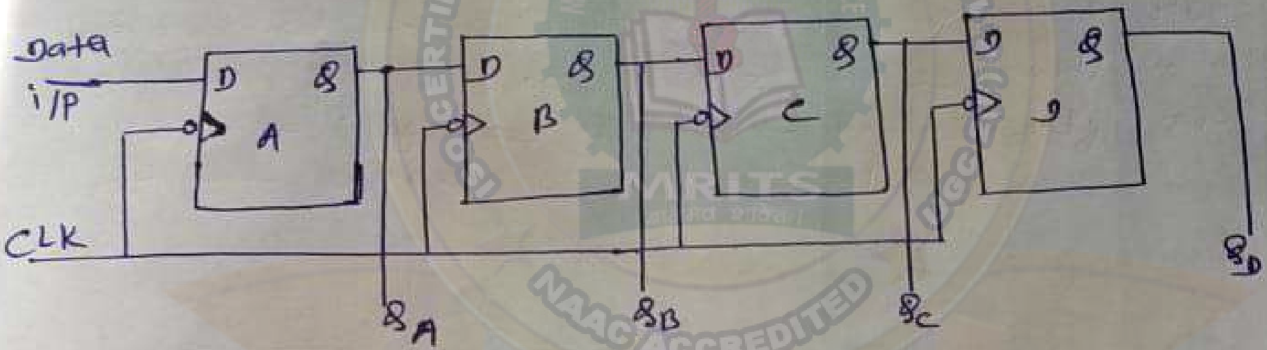
(ii) SIPO (Serial-In-parallel out):-

→ For 'n' bit serial input data to be stored, the number of CLK pulse required is n.

→ For 'n' bit parallel output data to be stored, the number of CLK pulse required is zero.

for example:-

A 4-bit Serial-In-parallel-out (SIPO) register is shown in fig(a). It consist of one serial input and outputs are taken from all the flip-flops are parallel. In this register, data is shifted serially but shifted out in parallel.



fig(a) 4-bit SIPO register.

(iii) PISO (parallel-In-Serial-Out) register:-

→ To store parallel in data, if we store n-bit then the number of CLK pulse required = 1 clock pulse

→ To store serial out data, if we store 'n' bit then the number of clock pulse required = (n-1).

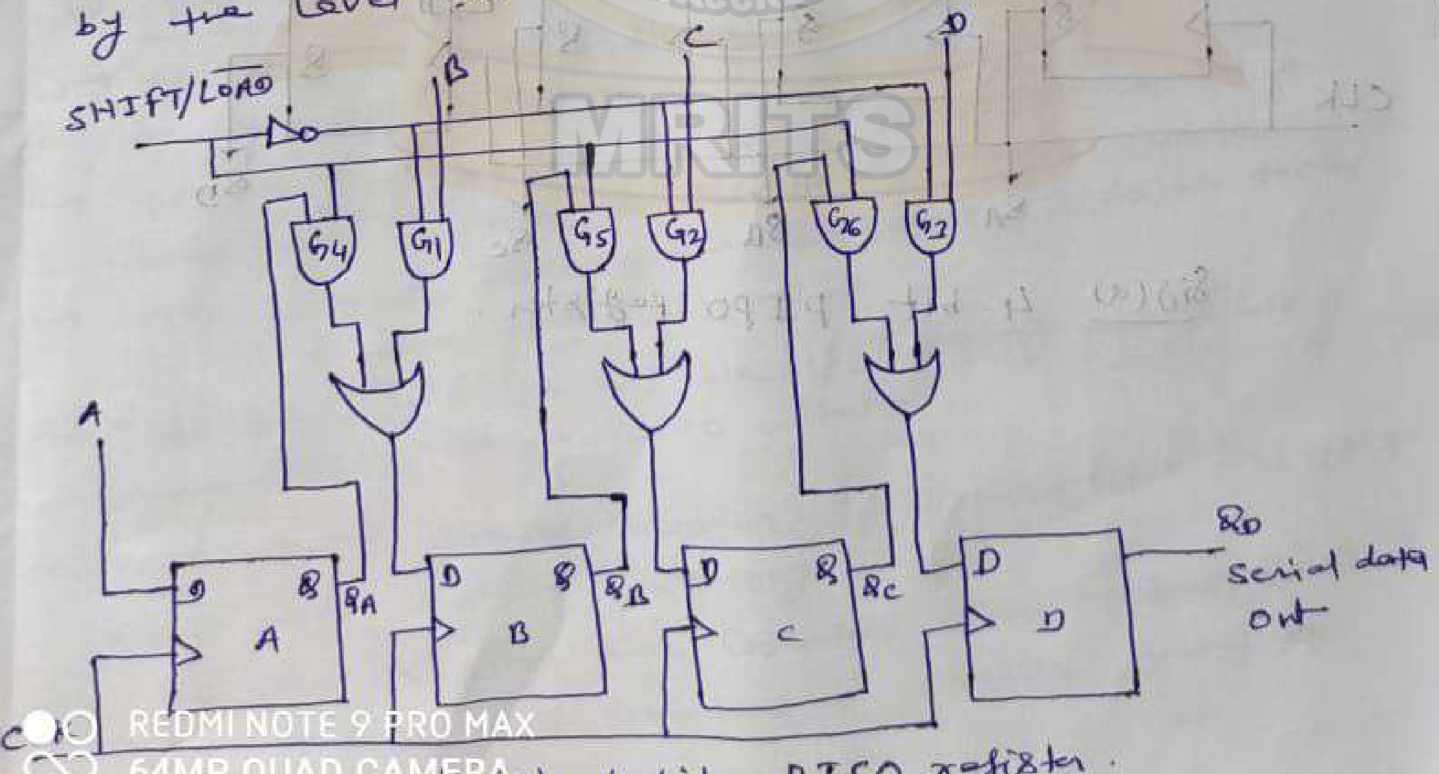
for example:-

A 4-bit PISO register is shown in fig(a).

Let A, B, C and D be the four parallel data input lines and SHIFT/$\overline{LOAD}$ is a control input that allows the four bits of data at A, B, C and D inputs to enter into the register in parallel or shift the data in serial.

→ when SHIFT/$\overline{LOAD}$ is LOW, AND gate G_1 through G_3 are enabled, allow the data at parallel input i.e. B, C and D to the D input of its respective flip flop. The A input is directly connected to the D input of the first flip-flop. When a clock pulse is applied, the flip-flop with D=1 will be SET and the flipflop with D=0 will be RESET. Thereby storing all four bits simultaneously.

→ when SHIFT/$\overline{LOAD}$ is HIGH, AND gates G_1 through G_3 are disabled and the remaining AND gates G_4 through G_6 are enabled, allow the data bits to shift right from one stage to the next. The OR gates allow either the normal shifting operation or the parallel data-entry operation, depending on which the AND gates are enabled by the level on the SHIFT/$\overline{LOAD}$ input.



fig(a) 4-bit PISO register.

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(iv) PIPO (Parallel-In-parallel-out) Register :-

→ For parallel-in data, the number of clk pulse required = 1 clk pulse

→ For parallel-out data, the number of clk pulse required = 0 clk pulse

→ A 4-bit PIPO register is shown in fig (a). In this register, data inputs can be shifted either in or out of the register in parallel. Also, in this register, there is no interconnection between successive flip-flops since no shifting is required. Here, the parallel inputs to be entered should be applied at A, B, C and D inputs which are directly connected to D input of respective flip-flop. On applying a clock pulse, these inputs are entered into the register and are immediately available at the output Q_A, Q_B, Q_C and Q_D.

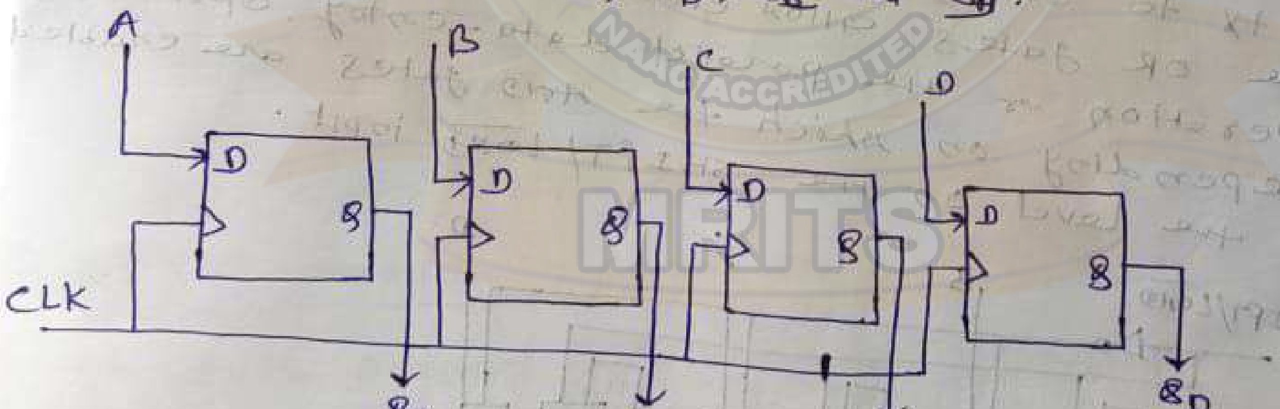


fig (a) 4-bit PIPO register.

⇒ Counters :-

→ It is a sequential circuit formed by the cascading of FFs.

→ Counters are basically used for
(i) Counting of the number of clock pulses required.
(ii) Frequency division
(iii) Timers
(iv) Frequency measurement
(v) Waveform generation

→ Counters are classified as:-
(i) Asynchronous Counter
(ii) Synchronous Counter

Notes :-
If N = Total no. of states and
n = number of flip-flops then
(i) If $N = 2^n$, then we get Binary Counter
(ii) If $N < 2^n$, then we get Non-binary Counter

⇒ MOD number :-

→ The "MOD number" indicates the number of states in counting sequence.

→ For n-FF, Counter will be 2^n different states and then this Counter is said to be MOD-2^n Counter.

→ MOD number indicates the frequency division factor obtained from the last FF.

→ It would be capable of counting upto $(2^n - 1)$ before returning to zero state.

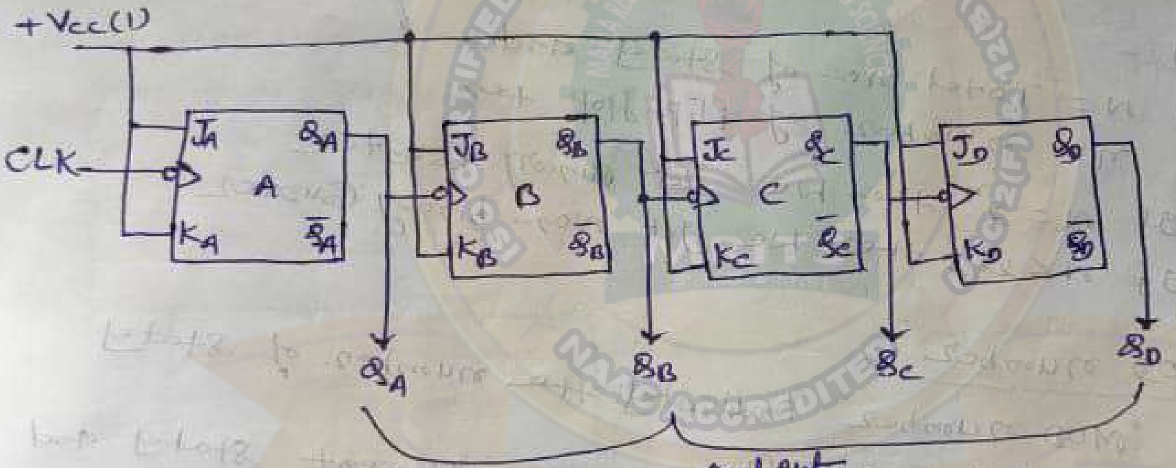
Note :- ① In MOD-N Counter, if applied input frequency is f, then output frequency is f/N.
(ii) If the counters are cascaded with MOD-M followed by MOD-N, then number of overall states of

Combined Counter is (MxN) and Counter is called "MOD-MN" Counter.

⇒ **Asynchronous (Series) Counter :-**

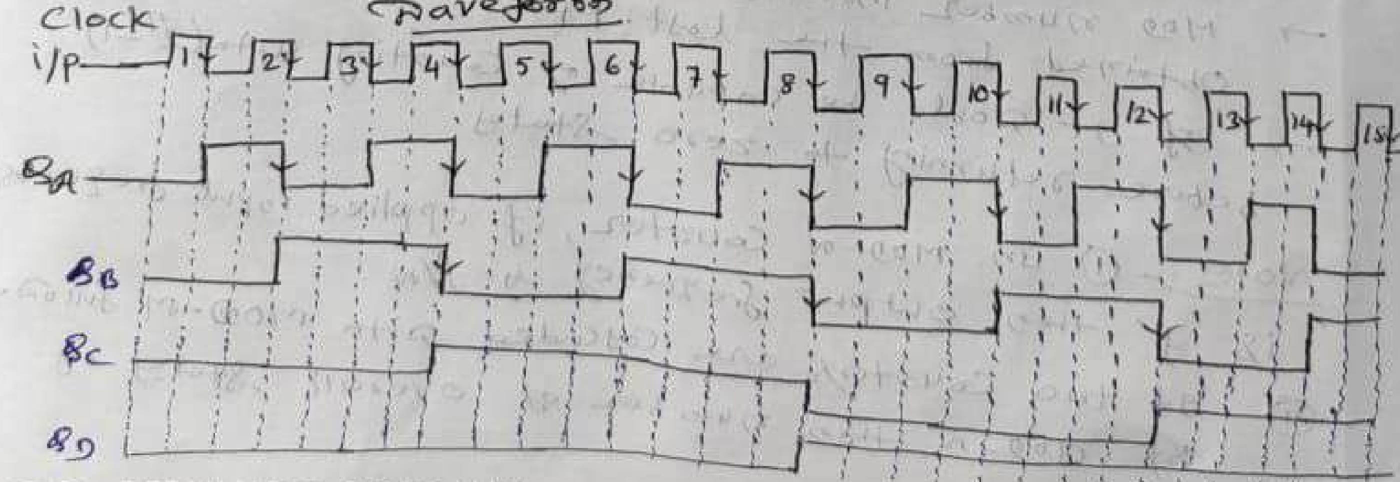
(i) **Binary Ripple Counter :-**

A 4-bit binary ripple Counter is shown in fig(a). A binary ripple Counter is constructed using clocked J-K ff. The system clock, a square wave, drives ff A. The output of A drives ff B, the output of B drives ff C and the o/p of C drives ff D. The overall propagation delay time of the Counter is the sum of individual delay of flip flop. All the J and K inputs are connected to Vcc (1), which means that each flip flop toggles on the negative edge of its clock i/p.



fig(a) 4-bit binary ripple Counter

Waveform



Truth - table:

State	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

Mod-number or modulus:-

It is a MOD-16 ripple counter.

- The MOD-number of a counter is the total number of states it sequences through in each complete cycle.

∴ MOD-number $= 2^n$

where n = no. of ff.

Max^n binary number counted by the counter is $2^n - 1$

Therefore 4-flip-flop counter can count $= 2^4 - 1 = 15_{10}$

⇒ Ripple Counters with Modulus $< 2^n$:-

Non-Binary Ripple Counter :-

- A MOD-6 ripple counter is shown in fig (b).

Here we take 3-flip-flop.

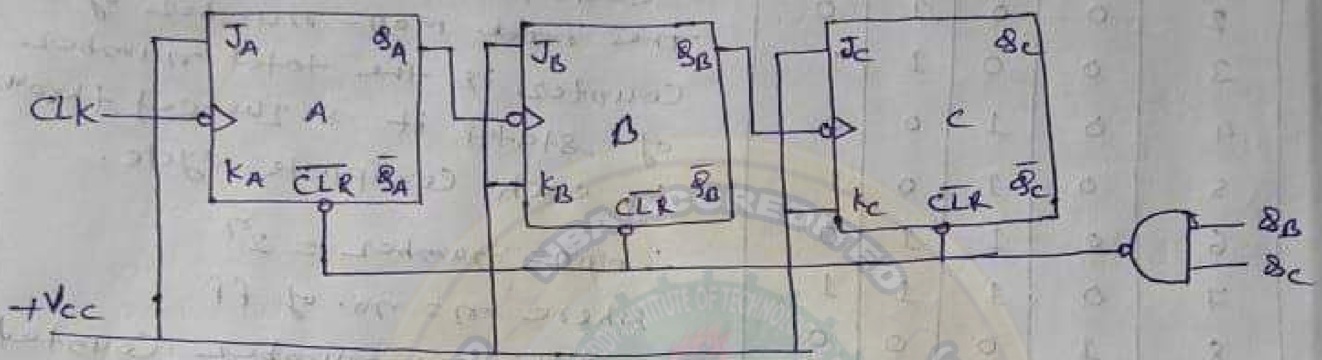
∴ No. of states $= 2^3 = 8$ states.

Used states = 6 and

Unused states = 2

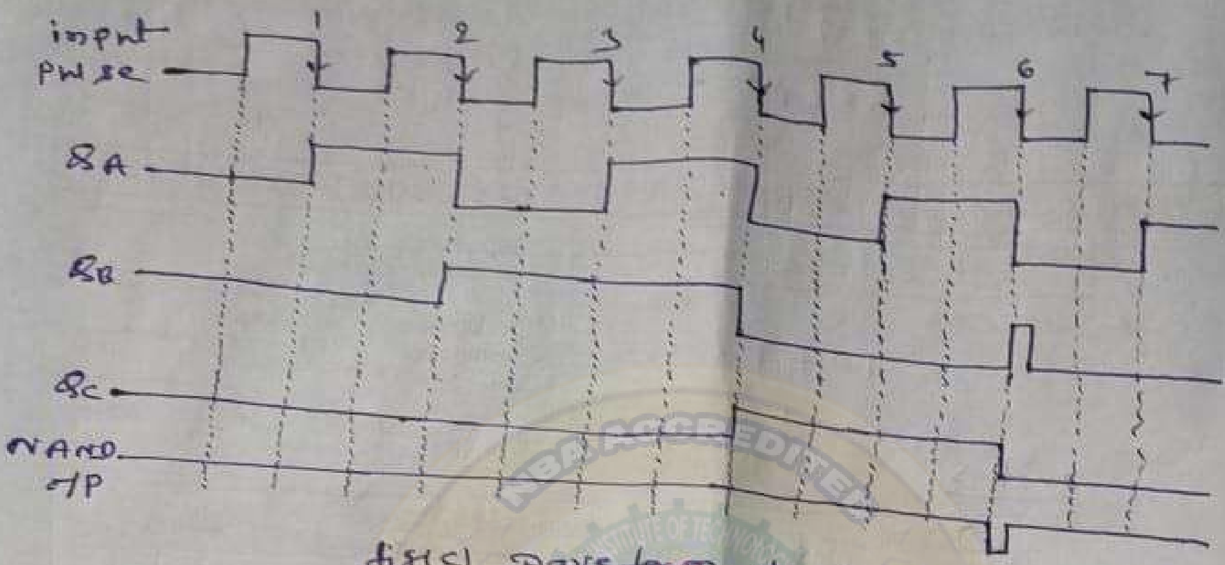
Output frequency of MOD-6 counter = $f/6$.

→ Clear (CLR) and preset is used in non-binary Counter.
→ Clear (CLR) is used to reset Counter without clock.
→ preset is used to set Counter.



fig(b) MOD-6 Ripple Counter.

1. NAND gate output is Connected to the clear inputs of each flip-flop. As long as the NAND gate output is HIGH, it will have no effect on the Counter. When the NAND gate output goes LOW, it will clear all flip-flop and the Counter immediately goes to the 000 state.
2. The outputs of Counter Q_B and Q_C are given as input to the NAND gate. The NAND gate output goes LOW whenever $Q_B = Q_C = 1$. This Condition will occur when the counter goes from the 101 state to the 110 state (i.e. 6th i/p pulse). The LOW at the NAND gate output will clear the Counter to the .000 state. Once the flip flop have been cleared, the NAND gate output goes back to HIGH, since $Q_B = Q_C = 1$ Condition no longer exist.
3. The Counting sequence is 000 → 001 → 010 → 011 → 100 → 101 → 000 → ---



fig(c) waveform of MOD-6 ripple counter.

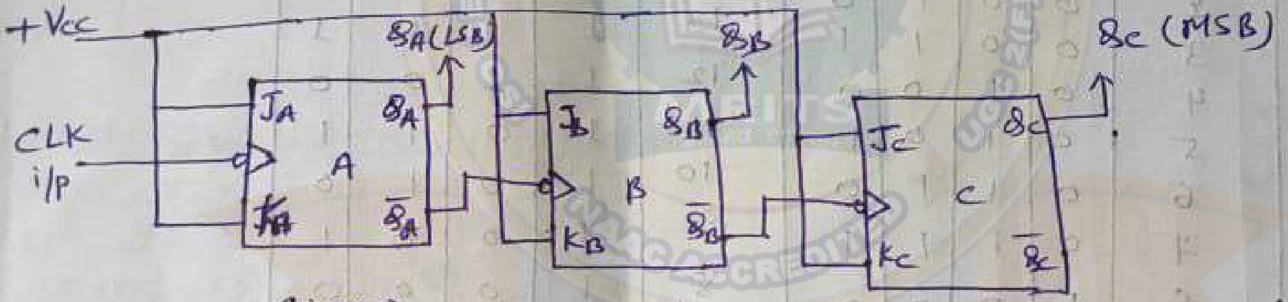
⇒ **Asynchronous Down Counter :-**

A down counter using n-FF counts downward from a maximum count of (2^n-1) to zero. The countdown sequence for a 3-bit down counter is shown in table.

State	Q_C	Q_B	Q_A
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0
7	1	1	1

Table 3-bit Asynchronous down counter.

The truth table shows that the output Q_A (LSB) changes its states (toggles) at each negative transition of clock as it does in the up-counter. The Q_B output changes state every time Q_A goes from LOW to HIGH. i.e. when $\overline{Q_A}$ goes from HIGH to LOW, Q_C changes state each time Q_B goes from LOW to HIGH, i.e. when $\overline{Q_B}$ goes from HIGH to LOW. Thus in a down counter, each flipflop, except the LSB flipflop, must toggle when the inverted output ($\overline{Q}$) of the preceding flipflop goes from HIGH to LOW. The fig(a) shows for a MOD-8 down counter.

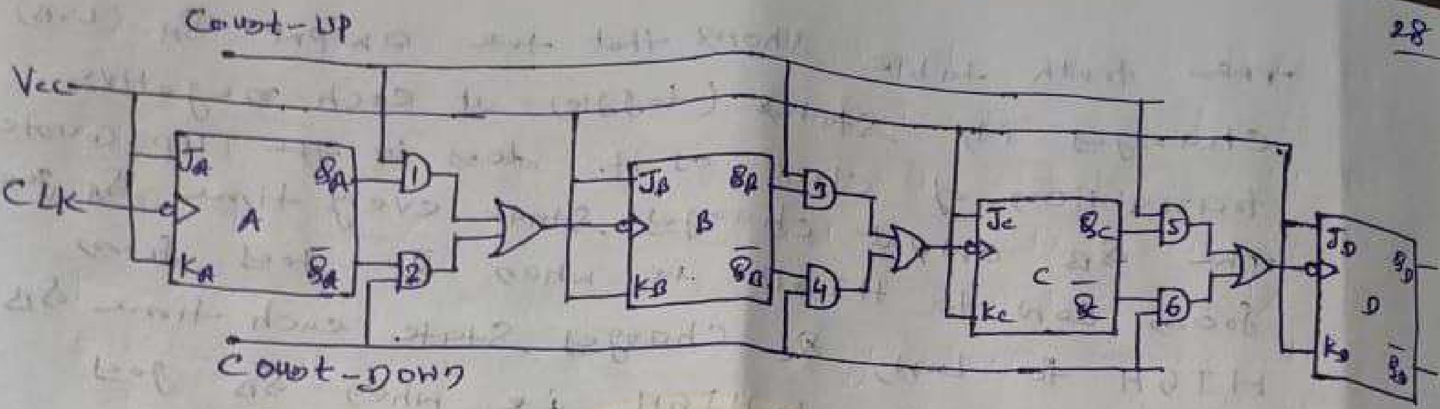


<u>fig(a)</u> MOD-8 down counter.

⇒ <u>Asynchronous UP-down Counter</u>.

UP-DOWN Counter is also called Multimode Counter.
In UP-Counter, each flip-flop is triggered by the normal output of the preceding flip-flop.
In a Down-Counter, each flip-flop is triggered by the inverted o/p of the preceding flip-flop.
In both the Counter, the first flipflop is triggered by the input pulse.

→ A 4-bit UP-DOWN Counter whose operation is controlled by the UP-DOWN control inputs is shown in fig(a).



Fig(a) Asynchronous 4-bit UP-DOWN Counter.

The Truth-table of 4-bit UP-DOWN Counter :-

Count-UP Mode					Count-DOWN Mode				
states	Q_D	Q_C	Q_B	Q_A	states	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0	15	1	1	1	1
1	0	0	0	1	14	1	1	1	0
2	0	0	1	0	13	1	1	0	1
3	0	0	1	1	12	1	1	0	0
4	0	1	0	0	11	1	0	1	1
5	0	1	0	1	10	1	0	1	0
6	0	1	1	0	9	1	0	0	1
7	0	1	1	1	8	1	0	0	0
8	1	0	0	0	7	0	1	1	1
9	1	0	0	1	6	0	1	1	0
10	1	0	1	0	5	0	1	0	1
11	1	0	1	1	4	0	1	0	0
12	1	1	0	0	3	0	0	1	1
13	1	1	0	1	2	0	0	1	0
14	1	1	1	0	1	0	0	0	1
15	1	1	1	1	0	0	0	0	0
0	0	0	0	0	15	1	1	1	1

⇒ Propagation delay in Ripple Counter:-

→ The main drawback of a ripple counter is that it has cummulative settling time. In ripple counter each flip-flop is triggered by the transition at the output of the preceding flip flop.

For proper operation of the ripple counter

$$T_{CLK} \geq n\, t_{pd(ff)}$$

and

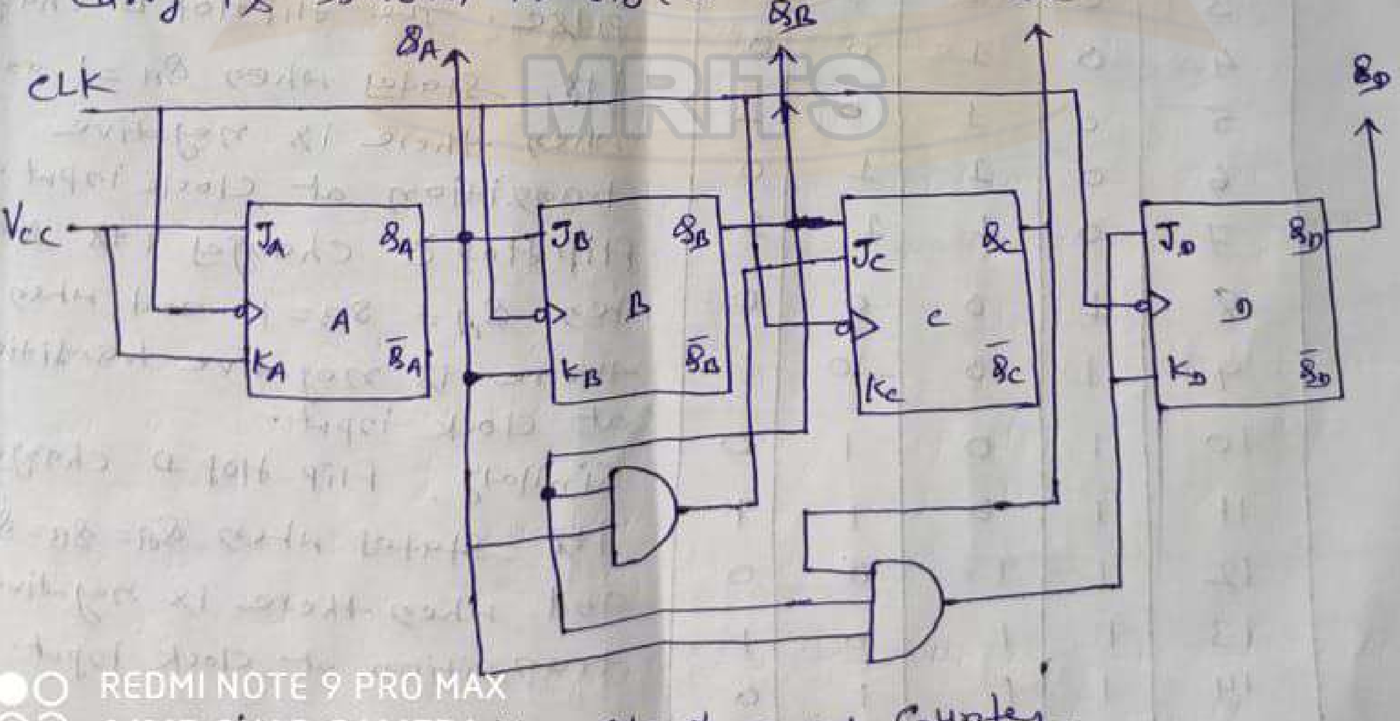
$$f_{CLK} \leq \frac{1}{n\, t_{pd(ff)}}$$

Maximum clock frequency is

$$f_{CLK(max)} = \frac{1}{n\, t_{pd(ff)}}$$

⇒ Synchronous (Parallel) Counter:-

A 4-bit (MOD-16) synchronous counter with parallel carry is shown in fig(a)



Fig(a) 4-bit synchronous counter

In this counter, the clock inputs of all flipflops are connected together so that the input CLK signal is simultaneously to each flipflop. Only the LSB flipflop A has its J and K inputs connected permanently to Vcc while the J and K inputs of other flip flops are driven by some combination of flip flop outputs. The J and K inputs of the flipflop B are connected with Q_A output of flipflop A. The J and K inputs of flipflop C are connected with AND operated output of Q_A and Q_B. Similarly, the J and K input of D flip-flops are connected with AND operated o/p of Q_A, Q_B and Q_C.

→ Truth table of 4-bit binary synchronous counter

state	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

from truth table,

flipflop A changes its state with the occurence of negative transition at each clock pulse. The flipflop B changes its states when $Q_A = 1$ and when there is negative transition at clock input. flipflop C changes its state when $Q_A = Q_B = 1$ and when there is negative transition at clock input.

Similarly, flip-flop D changes its states when $Q_A = Q_B = Q_C = 1$ and when there is negative transition at clock input.

→ Total delay = propagation delay of one flipflop + propogation delay of AND gate.

→ The maximum frequency of operation of synchronous counter is

$$f_{max} = \frac{1}{t_p + t_g}$$

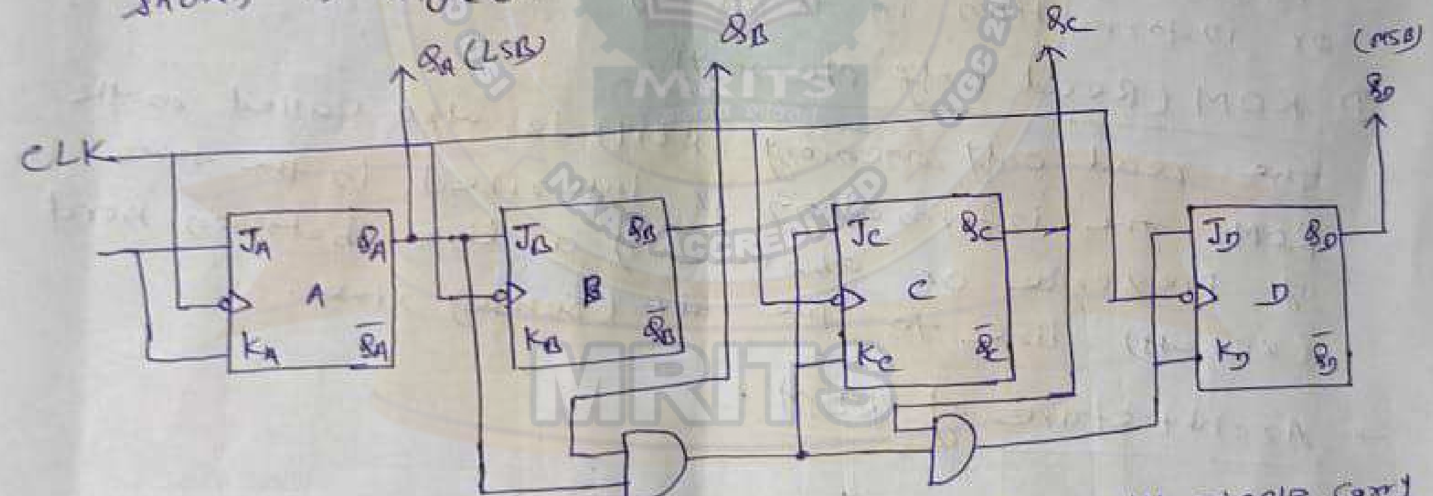
where t_p is propogation delay of one flipflop.

t_g is the propogation delay of one AND gate.

→ The synchronous counter has more complex circuitry than an Asynchronous counter.

⇒ <u>Synchronous counter with Ripple carry</u>:-

A 4-bit synchronous counter with parallel carry is shown in fig(b).



fig(b) 4-bit synchronous counter with ripple carry

→ The maximum clock frequency for a 4-bit synchronous counter with parallel carry is

$$f_{max} = \frac{1}{t_p + t_g}$$

In this counter, as the number of stages in a synchronous counter with parallel carry increases, the flip-flop must drive an ever increasing number of AND gates.

Similarly, the number of inputs per control gate also increases. The above problems of synchronous counter with parallel carry are eliminated in a ripple carry synchronous counter as shown in fig (b), but maximum clock frequency of the counter is reduced.

The maximum clock frequency for an n-bit synchronous counter with ripple carry is given by

$$f_{max} = \frac{1}{t_p + (n-1)\,t_g}$$

where,

n = no. of flipflop stages.

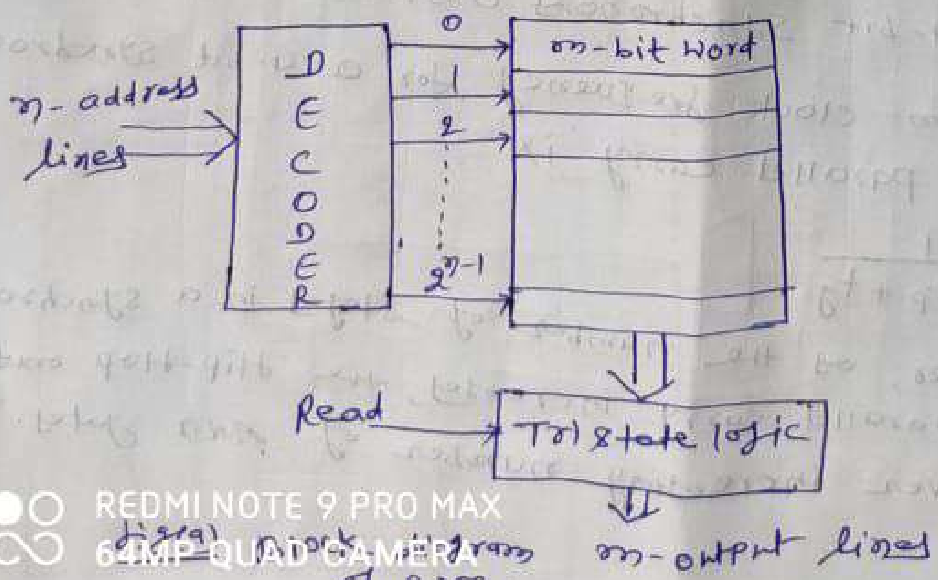
⇒ **Memory Devices:-**

Memories are devices that can store digital data or information in terms of bits.

① **ROM (Read only Memory):-**

The read only memory (ROM) is also called mask ROM. The information is inscribed in the form of presence or absence of a link between word (access) line to the bit (sense) line.

→ **Architecture of ROM:-**

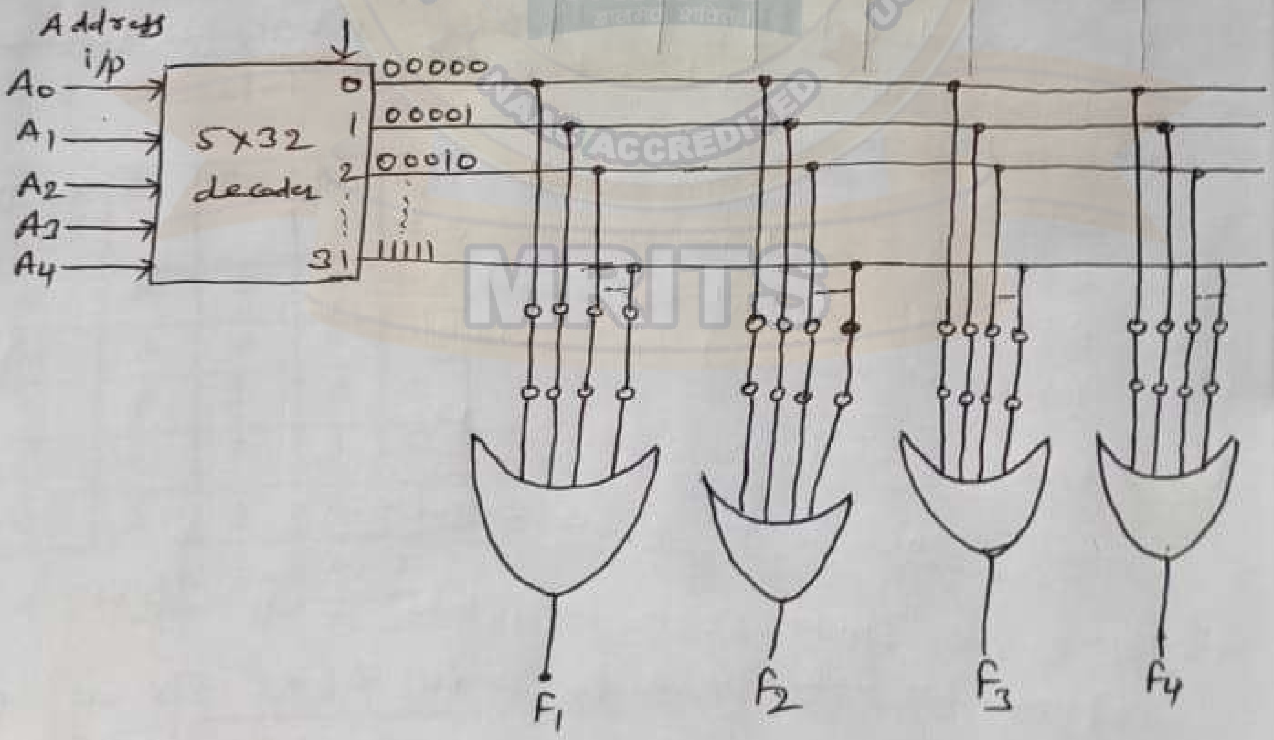


fig(a) block diagram of ROM.

The block diagram of ROM is shown in fig(a). It consists of n address lines and m output lines. Each bit combination of the address variables is called an address. Each bit combination that comes out of the output lines is called a data word. Hence the number of bits per word is equal to the number of output lines (m).

⇒ 32×4 ROM using OR gates:-

Internally, the ROM is a combinational circuit with AND gates connected as decoders and no. of OR gates is equal to the number of output lines in the unit. The internal logic construction of a 32×4 ROM is shown in fig(b).



fig(b) 32×4 ROM using OR gates

The 5 input variables are decoded into 32 ($2^5 = 32$) lines by means of 32 AND gates and 5 inverters. each one of the 32 address selects one and only one output of the decoder. The 32 outputs of the decoder are connected through fuses to each OR gate. Actually each OR gate has 32 inputs and each input of the OR gate goes through a fuse that can be blown as desired.

⇒ Types of ROM :